NTUEE Undergraduate Semi-Lab Fabrication and Characterization of Schottky MOSFET

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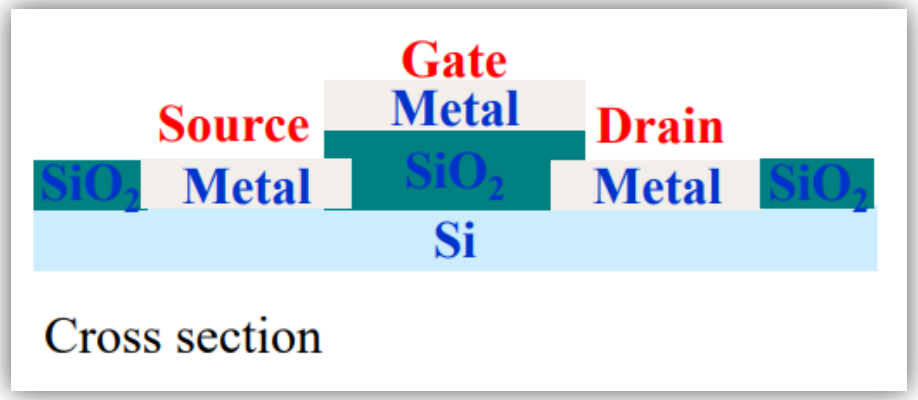
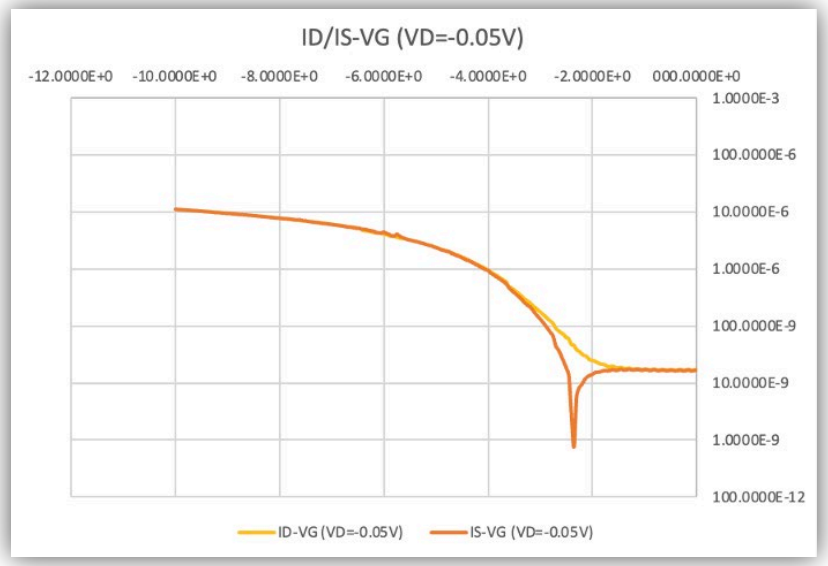
Goal

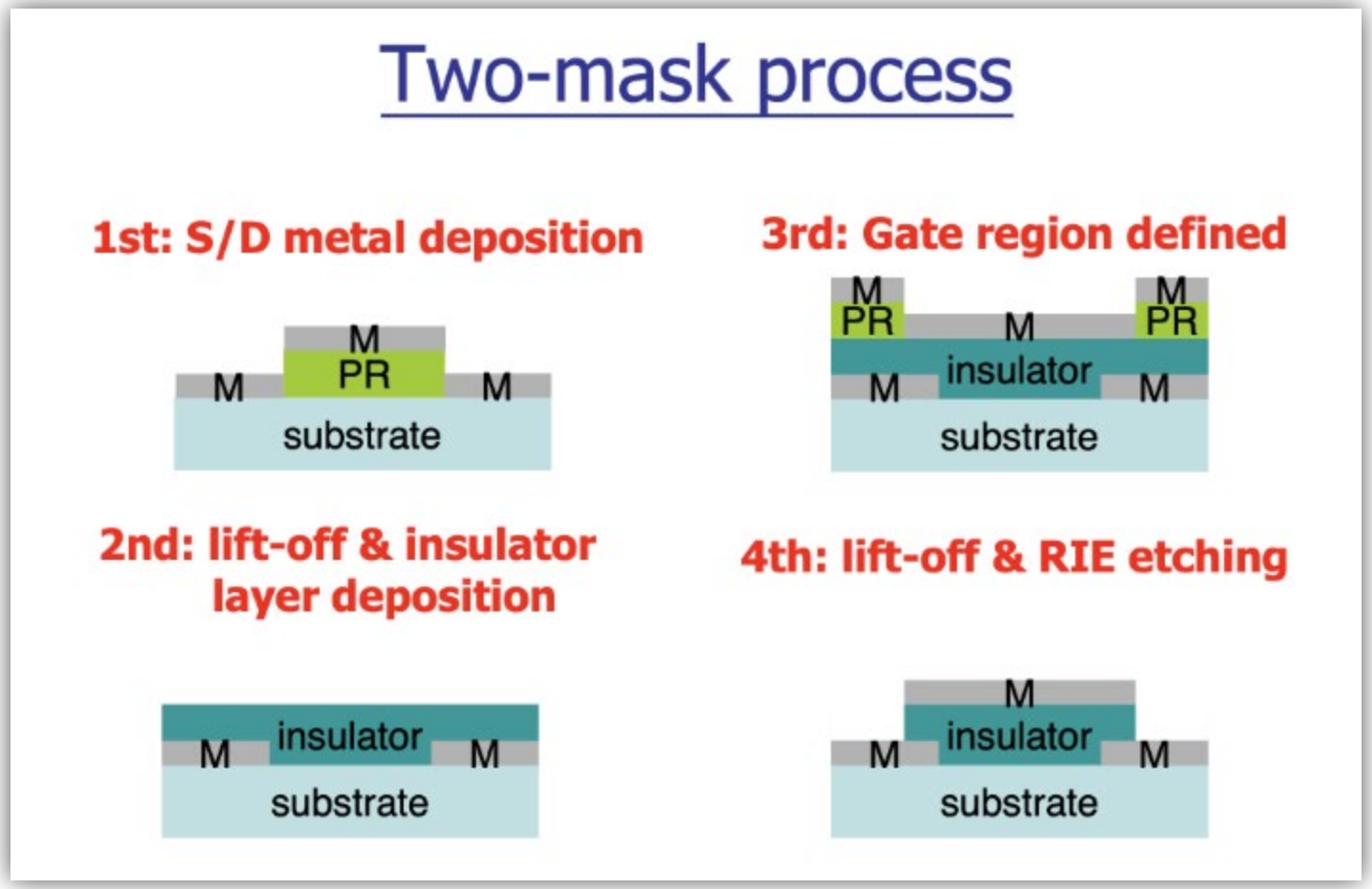
- To implement a Schottky MOSFET



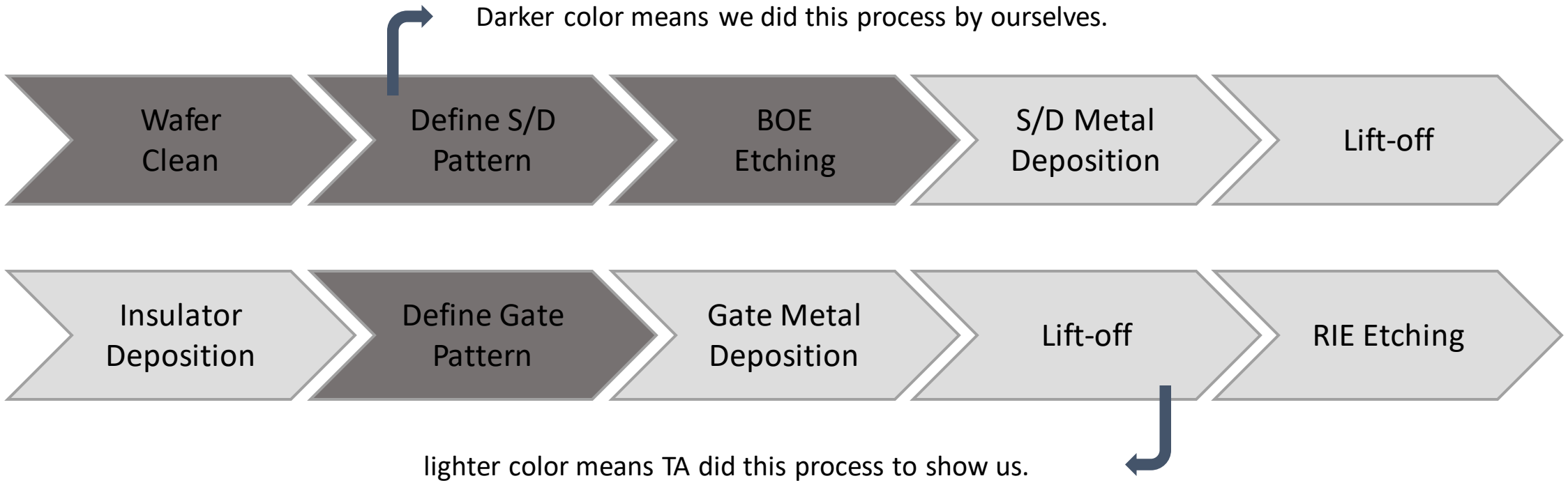
- To measure MOSFET's characterization



Process

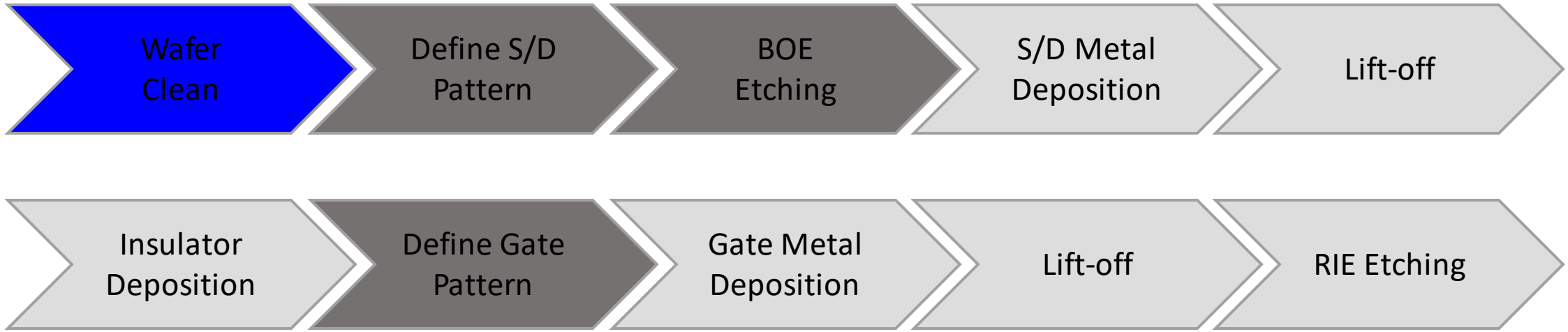

Two-mask process
1st: S/D metal deposition
M
PR
M
M
substrate
3rd: Gate region defined
M
M
PR
M
PR
insulator
M
M
substrate
2nd: lift-off & insulator layer deposition
insulator
M
M
substrate
4th: lift-off & RIE etching
M
insulator
M
M
substrate

Process Flow



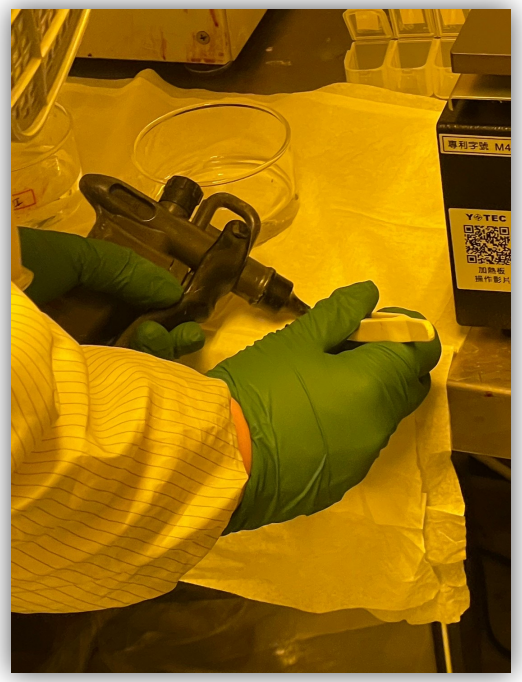
Process Flow

Blue is current process



Experimental Procedure – Clean Wafer

1. Dipping the sample in acetone to do ultra-sonic cleaning (3 minutes)
2. Dipping the sample in methanol to do ultra-sonic cleaning to wash acetone away (3 minutes)
3. Rinsing the sample by DI water (1 minute)
4. Etching the native oxide with BOE
5. Cleaning the sample by N_2 spray gun

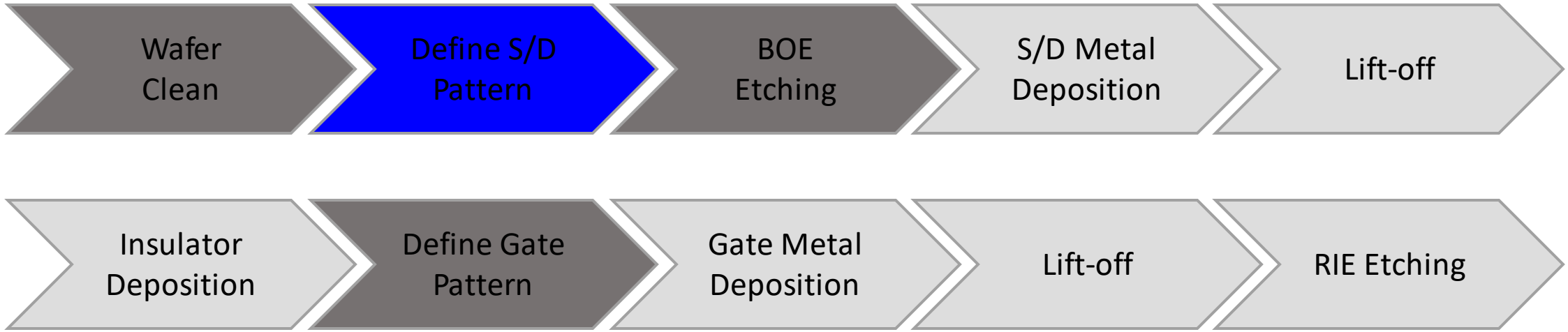


Acetone: http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/cleaning/%E4%B8%99%E9%85%AE.pdf

BOE: Buffered Oxide Etchant http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/etching/wet%20etching/1.pdf

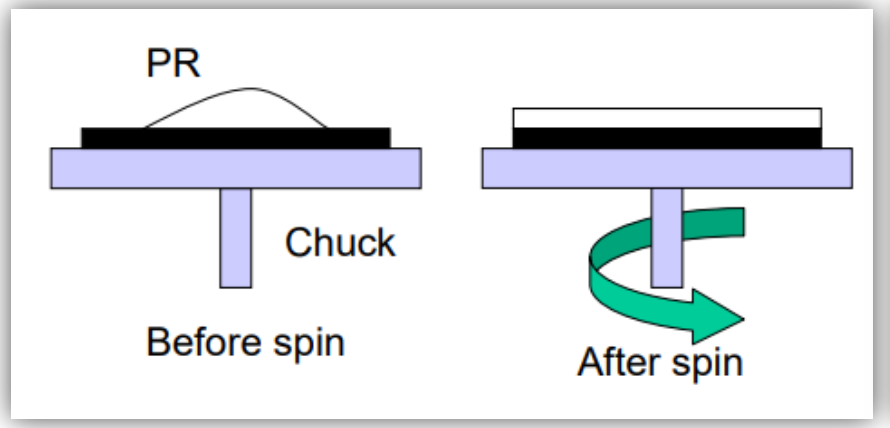
Process Flow

Blue is current process



Experimental Procedure – Define S/D pattern

1. Photoresist coating
   - Put the sample on the PR coater, doing spinning check.
   - After checked, drip PR on the sample and spin it.

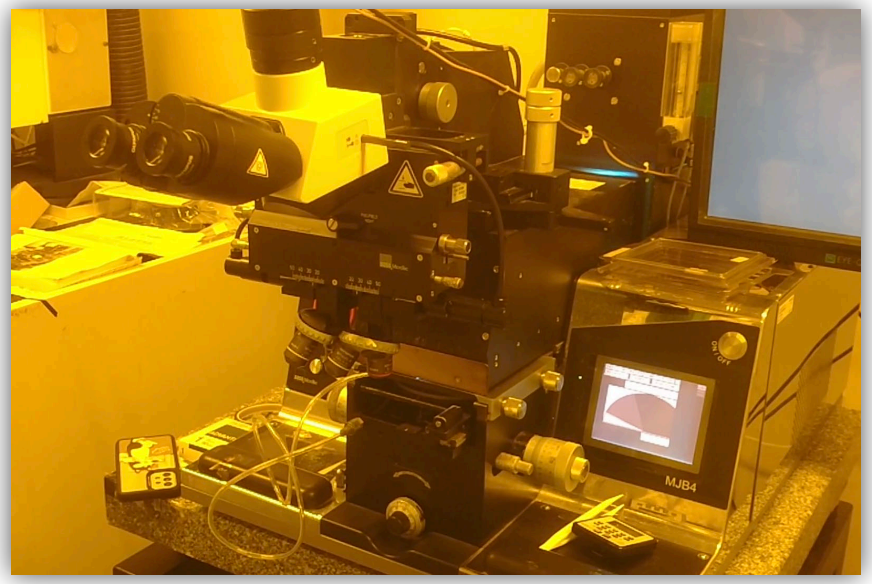


PR: photo resist AZ5214E http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/lithography/AZ5214E.pdf

Experimental Procedure – Define S/D pattern

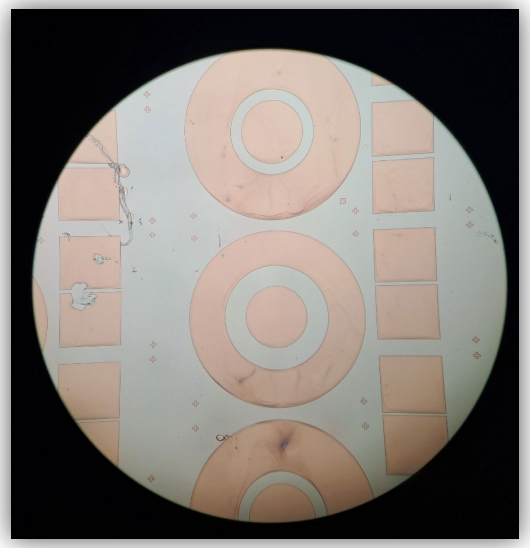
2. Soft bake
   - Put sample on the hot-plate (95˚C，3 min)
3. Exposure
   - Place the mask (with the plated side faces the sample)
   - Place the sample
   - Alignment: align the sample and mask
   - Exposure for 16 seconds

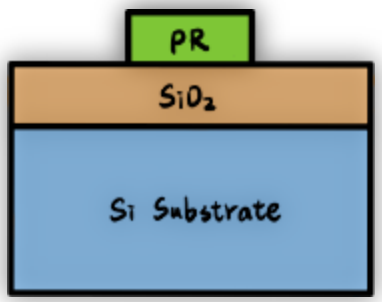
     (Hg lamp, i-line wavelength: 365nm, 260mW)



Experimental Procedure – Define S/D pattern

4. Blanket-bake & Exposure
   - Put the sample on the hot-plate (105˚C，35sec)
   - Exposure 30sec (Hg lamp, i-line wavelength: 365nm, 260mW)
5. Developing
   - Put the sample into developer liquid (MF-319)
   - Dipping in DI water for 15 sec, use N2 spray gun to dry the sample

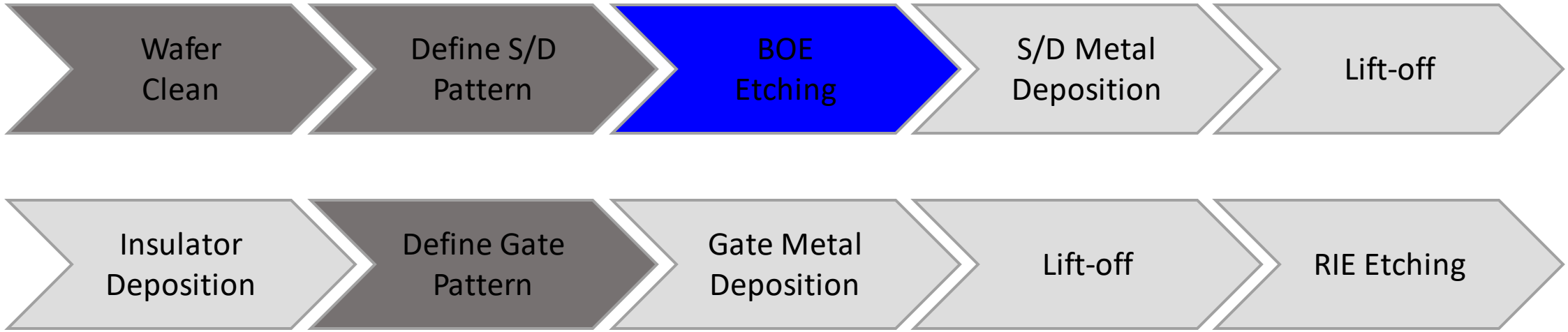




Developer: MF-319 http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/lithography/MF-319_developer.pdf

Process Flow

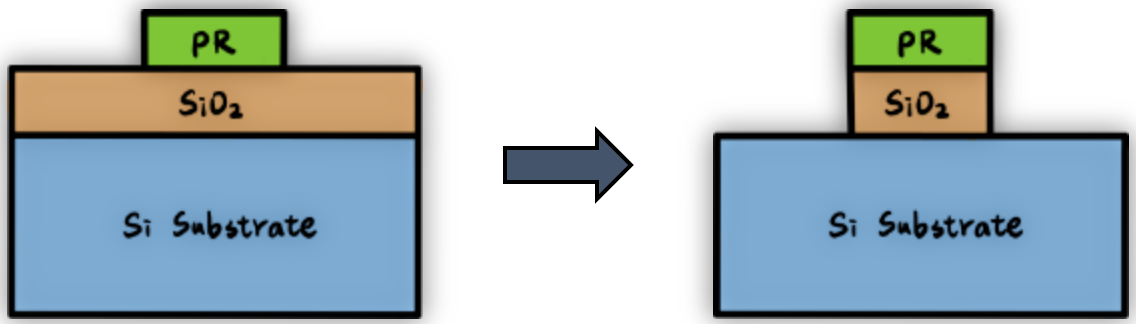
Blue is current process



Experimental Procedure – Etching

1. BOE Etching
    - Put the sample into the BOE liquid
2. Rinsing the sample by DI water
3. Cleaning the sample by N2 spray gun

Etching

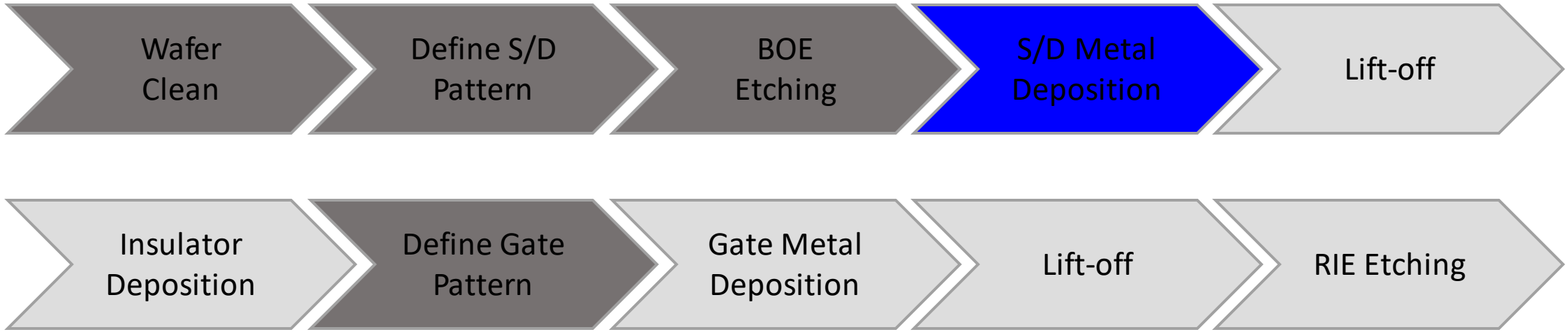


- Oxide wet etching
  - HF is commonly used for silicon dioxide wet etch
  - To slow down the oxide etch for better control of etch rate and uniformity, HF is further diluted in some buffer solution, such as NH4F
  - 6:1 BOE = 49% HF aqueous solution and 40% aqueous solution mix at the volume ration of 1:6 => use plastic or teflon container (glass will be etched)
  - The chemical reaction of oxide wet etching is

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O$$

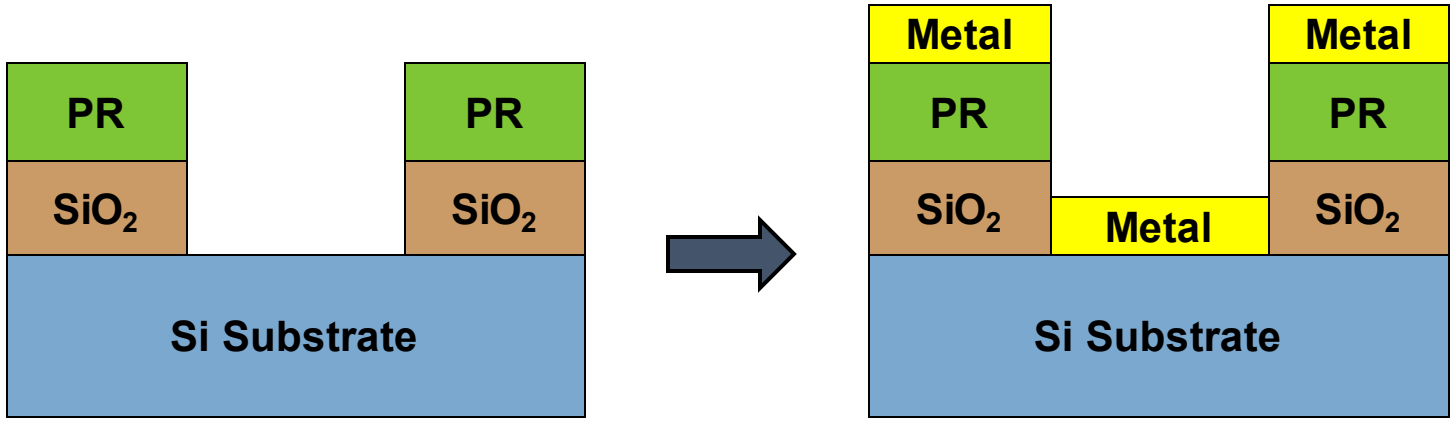
Process Flow

Blue is current process



S/D Metal Deposition

Sputter Machine



- S/D Metal Deposition

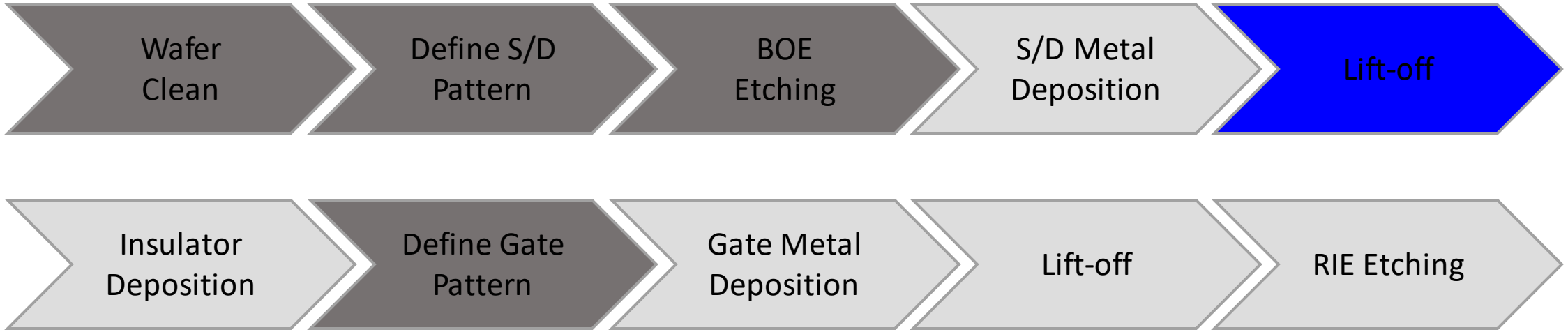
  →Metal is deposited by sputtering.

  →Metal directly contact to Si substrate to **form Schottky contact** In S/D hole.

  →PFET using Pt and NFET using Ti.

Process Flow

Blue is current process

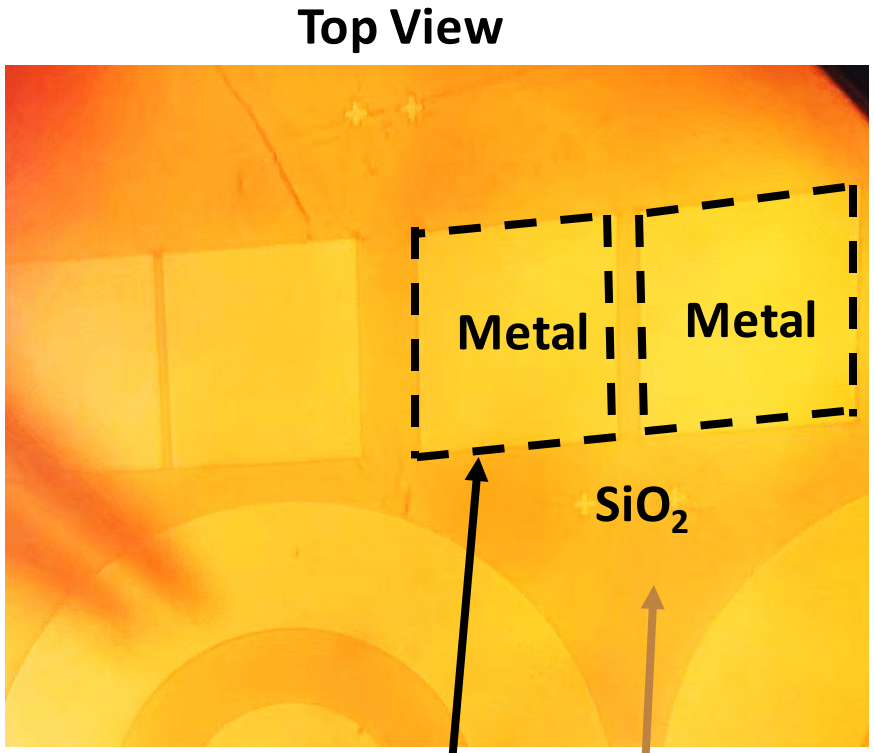


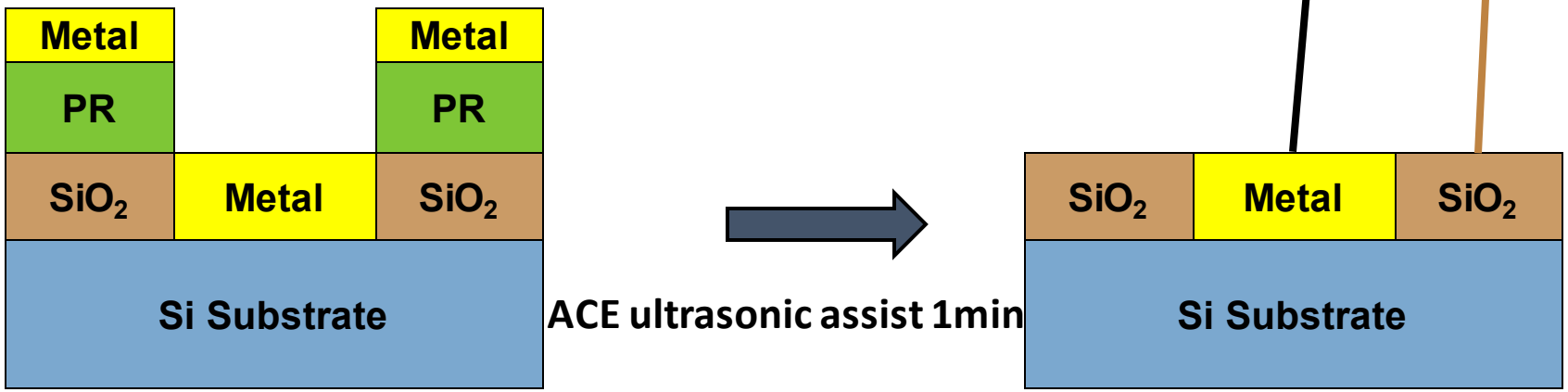
Lift off

- Lift off using acetone

→ Using acetone to dissolve PR

→ Leaving the metal in S/D hole

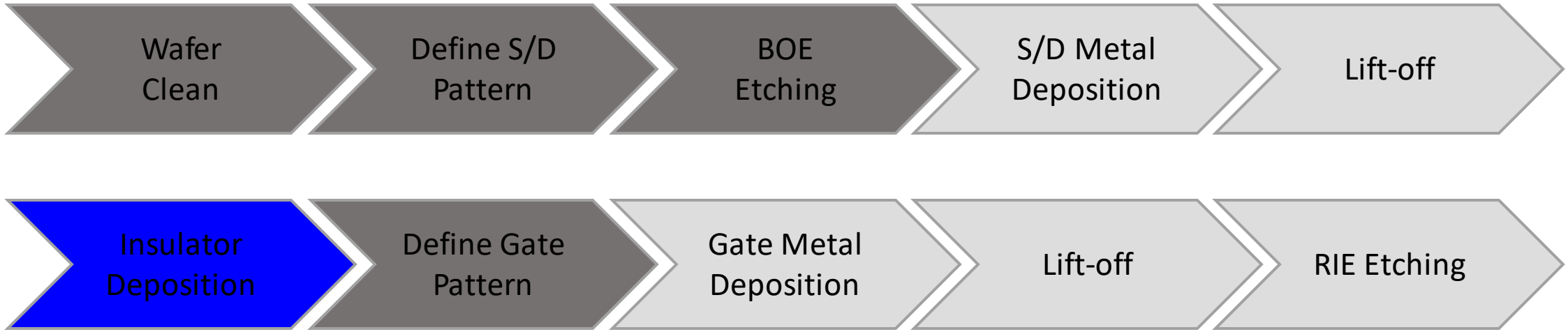




Acetone: http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/cleaning/%E4%B8%99%E9%85%AE.pdf

Process Flow

Blue is current process

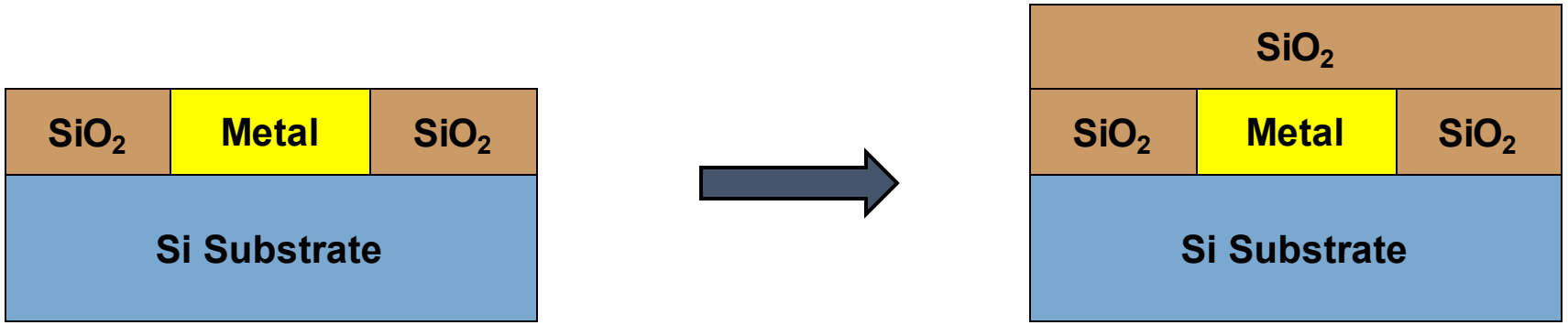


Insulator Deposition

- Grow SiO_2 using PECVD

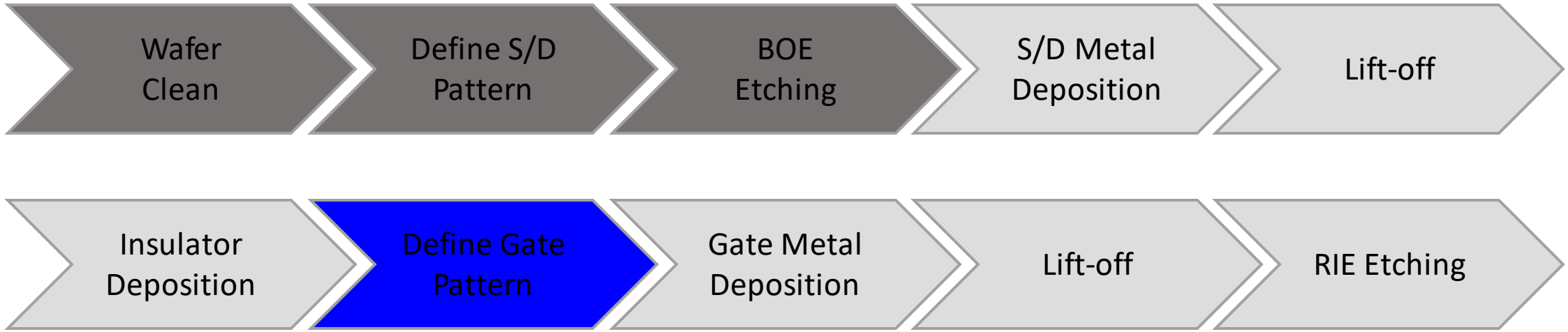
→Making S/D metal isolate with gate metal

→Prevent Gate to S/D current through the overlap region



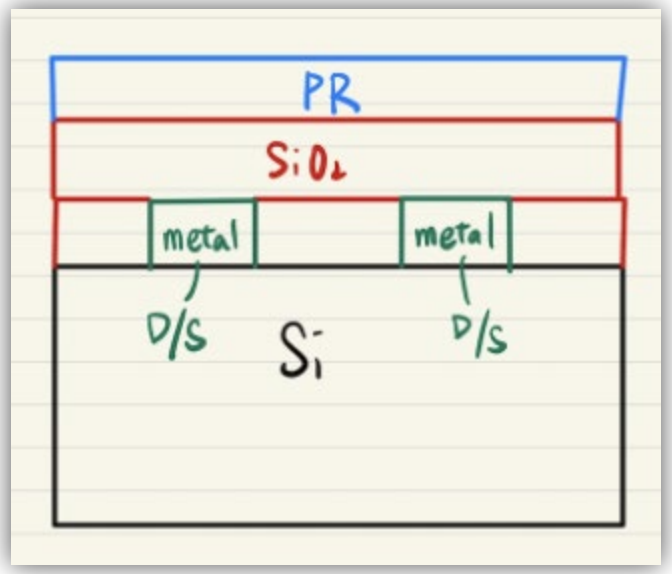
Process Flow

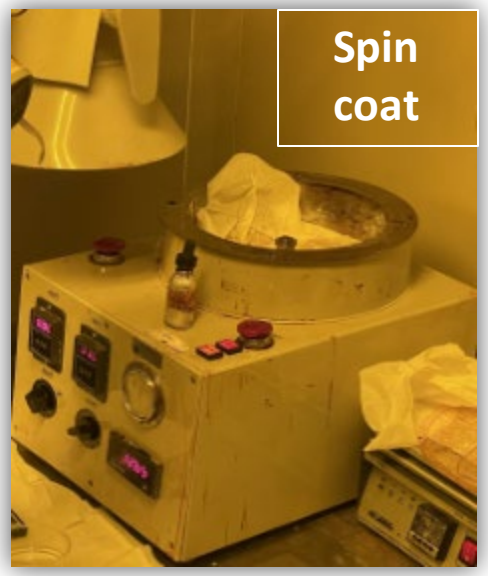
Blue is current process



Experimental Procedure – Define Gate Pattern

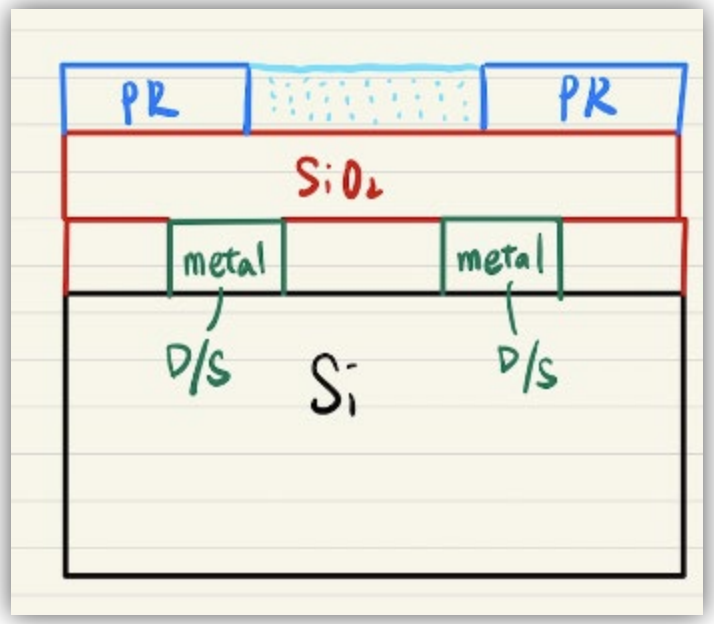
1. Spin coating
   - Spin coater: 1000 spins 10sec / 4000 spins 40sec
   - Soft bake: 95°C 3 minutes

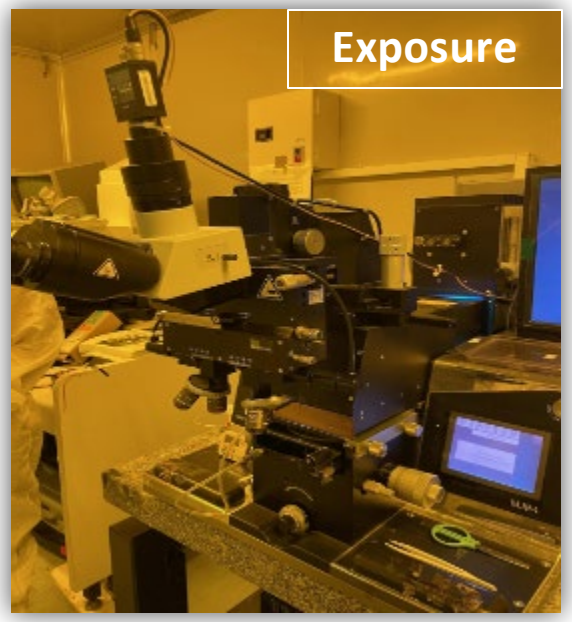




Experimental Procedure – Define Gate Pattern

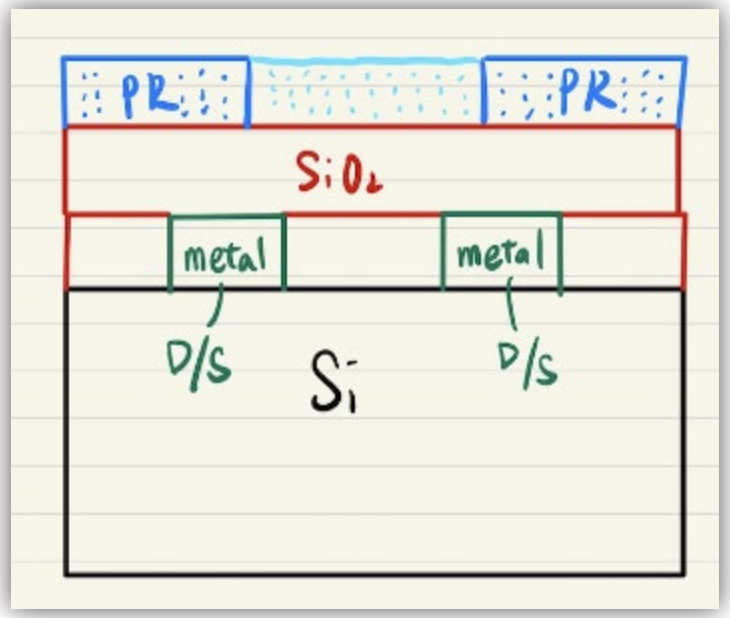
2. Alignment & Exposure
   - Mask: Cr metal
   - Exposure: 16 seconds (Hg lamp, i-line wavelength: 365nm, 260mW)

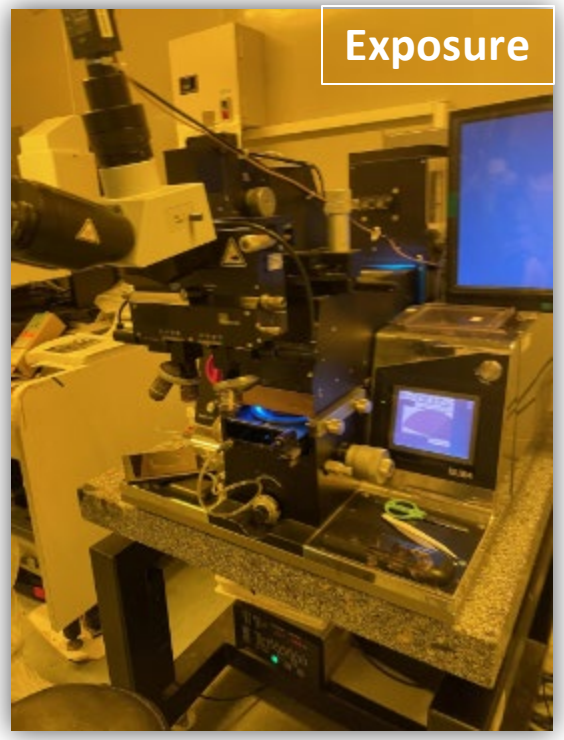




Experimental Procedure – Define Gate Pattern

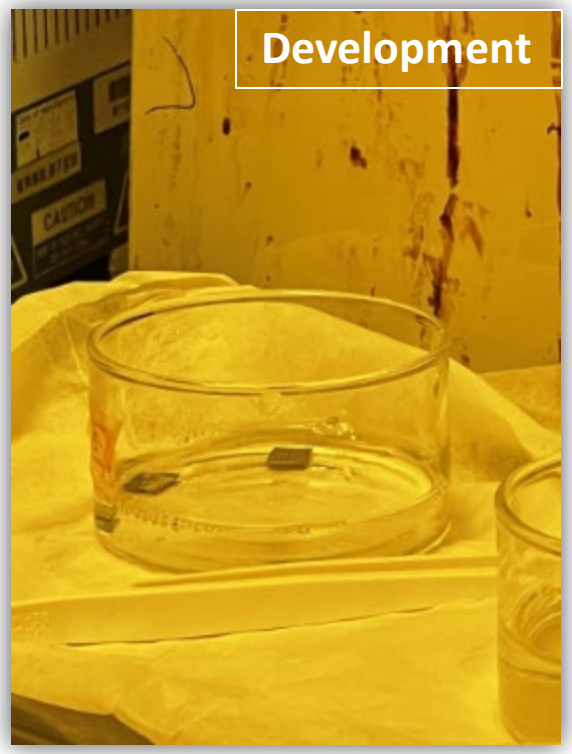
3. Blanket-bake & Exposure
   - Post-exposure bake: change the chemical property of the photoresist 105°C 35 seconds
   - Exposure: 30 seconds





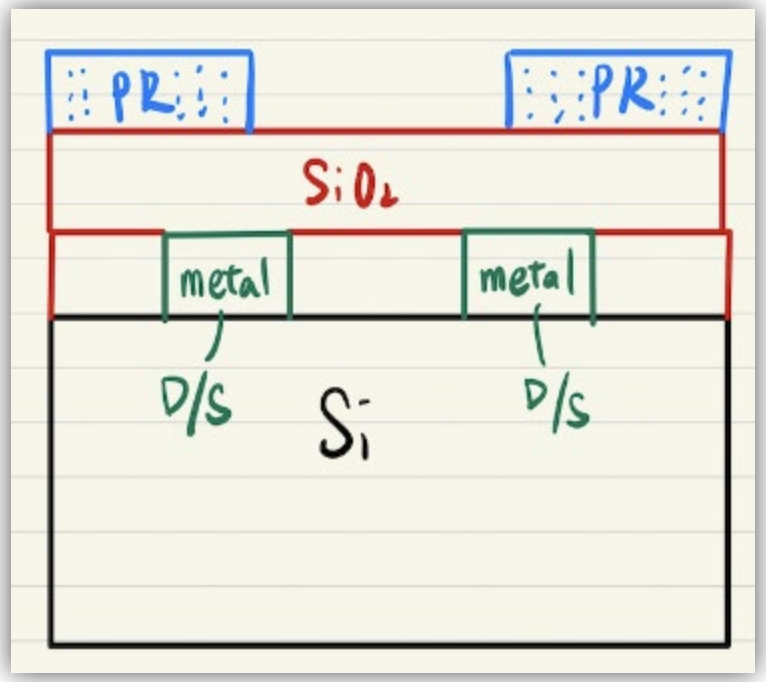
Experimental Procedure – Define Gate Pattern

4. Development

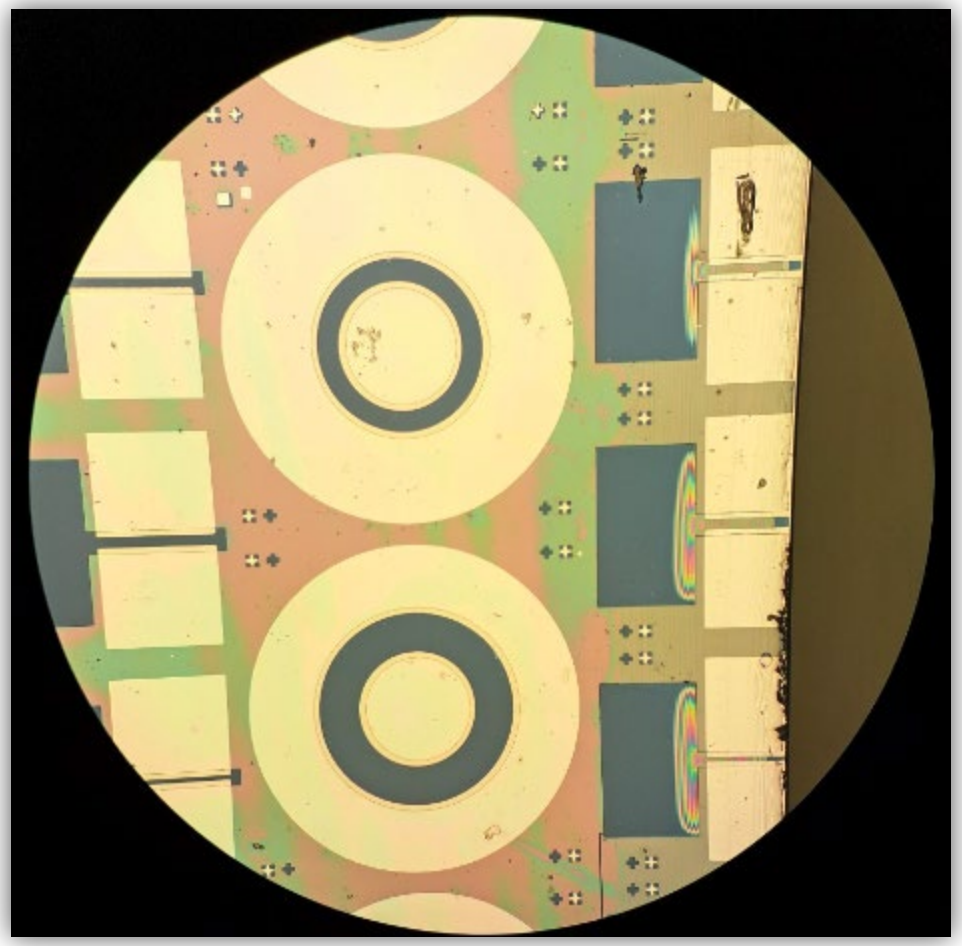


Experimental Procedure – Define Gate Pattern

4.
Development

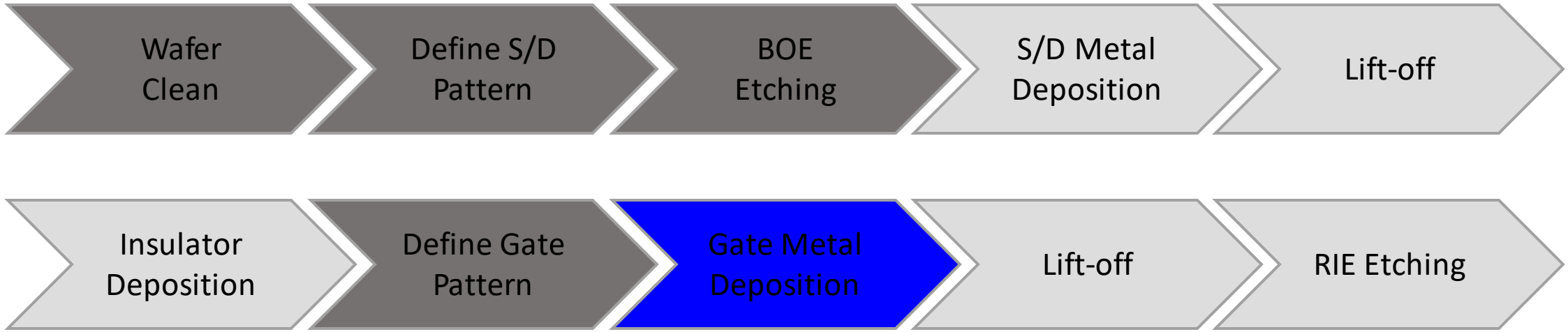


Experimental Result



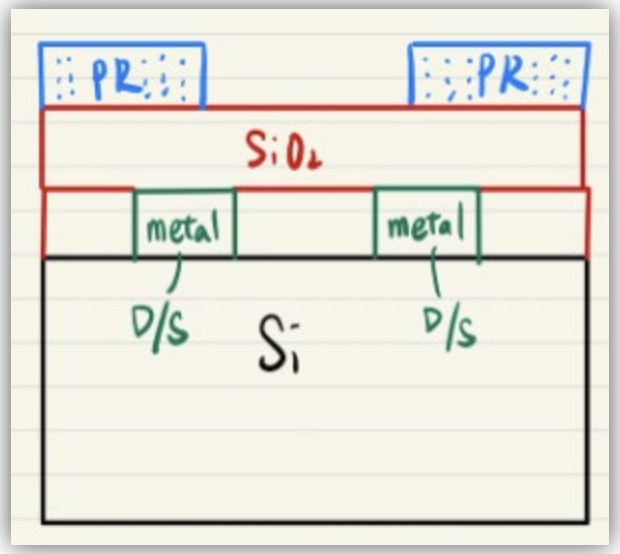
Process Flow

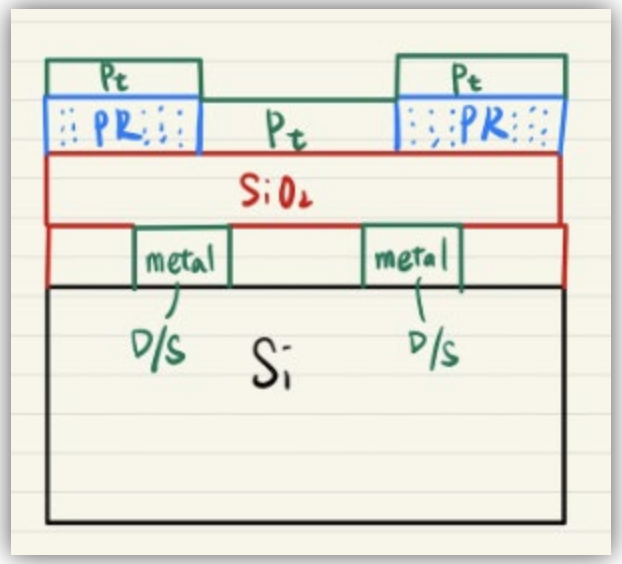
Blue is current process



Gate Metal Deposition

Sputter Machine



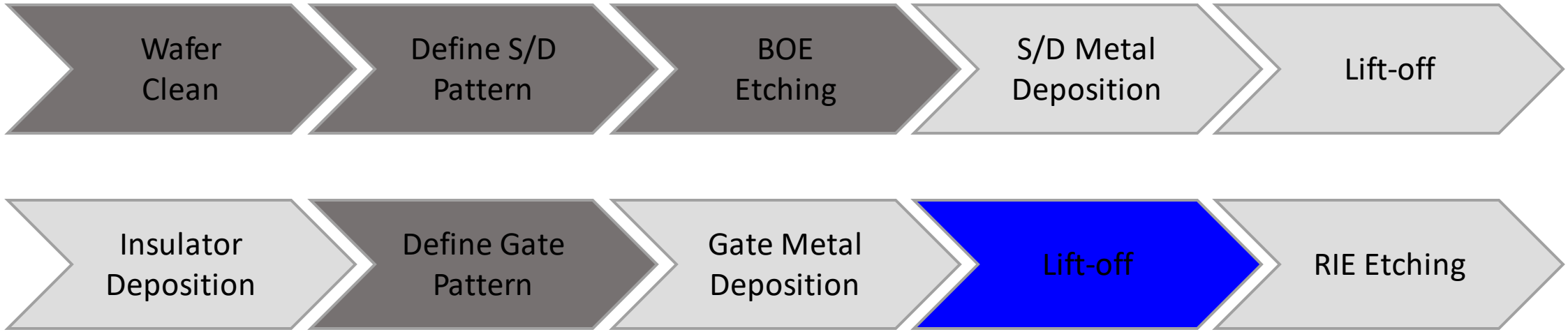


- Gate Metal Deposition

→Same as S/D Metal deposition.

Process Flow

Blue is current process

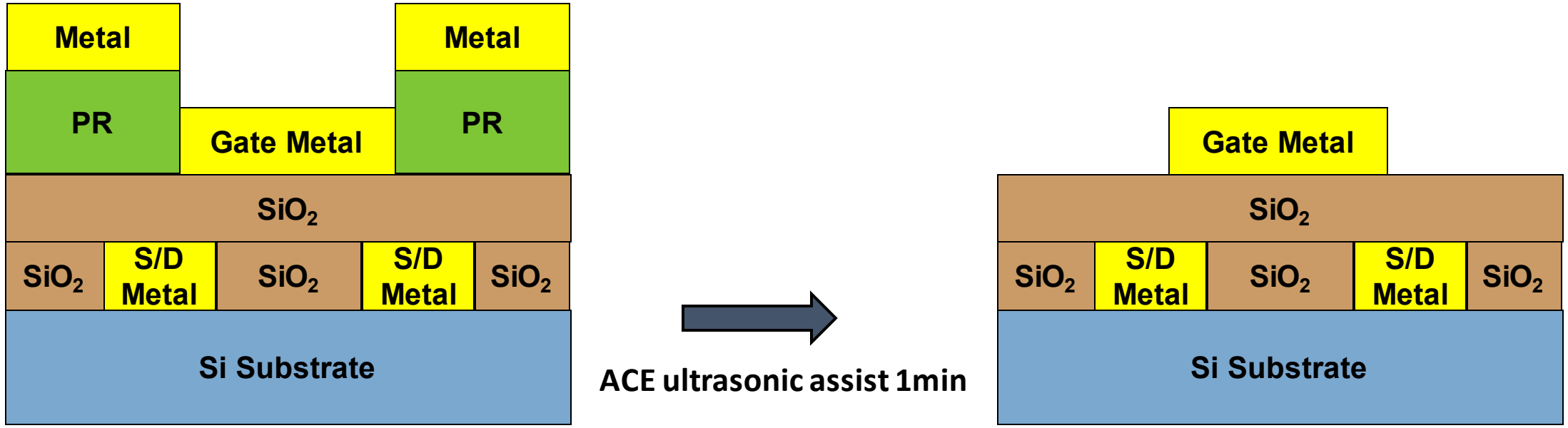


Lift off

- Lift off using acetone

→ Same as previous

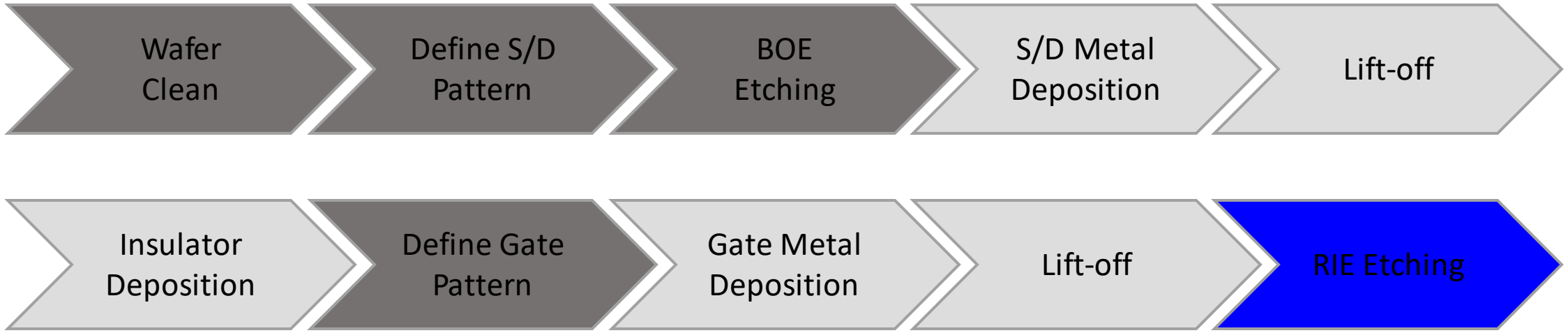
→ Leaving the metal in gate region as gate metal



Acetone: http://nanosioe.ee.ntu.edu.tw/semilab/MSDS/cleaning/%E4%B8%99%E9%85%AE.pdf

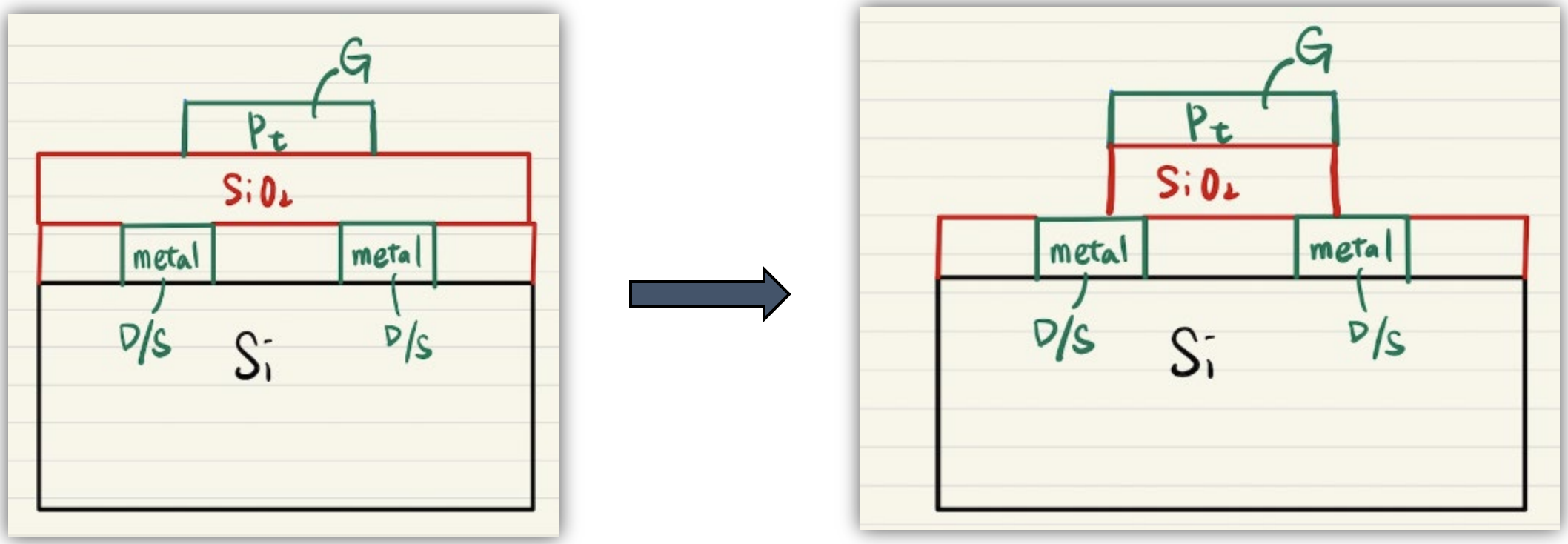
Process Flow

Blue is current process



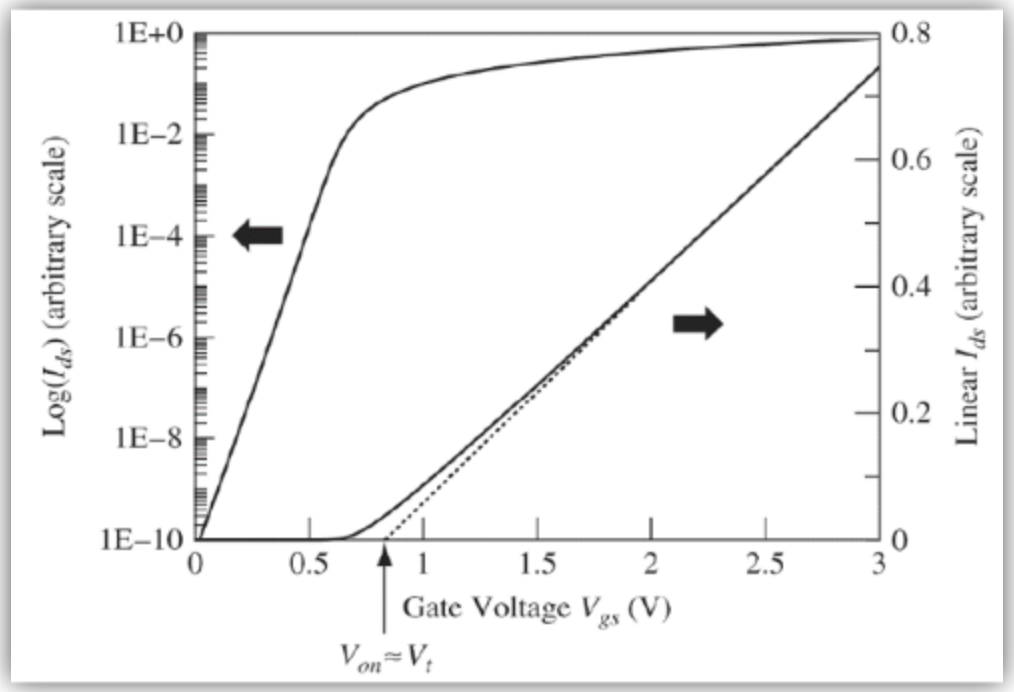
RIE etching

- RIE for etching the SiO_2 upon the S/D for measuring



Characterization Calculation

- Threshold Voltage V_T



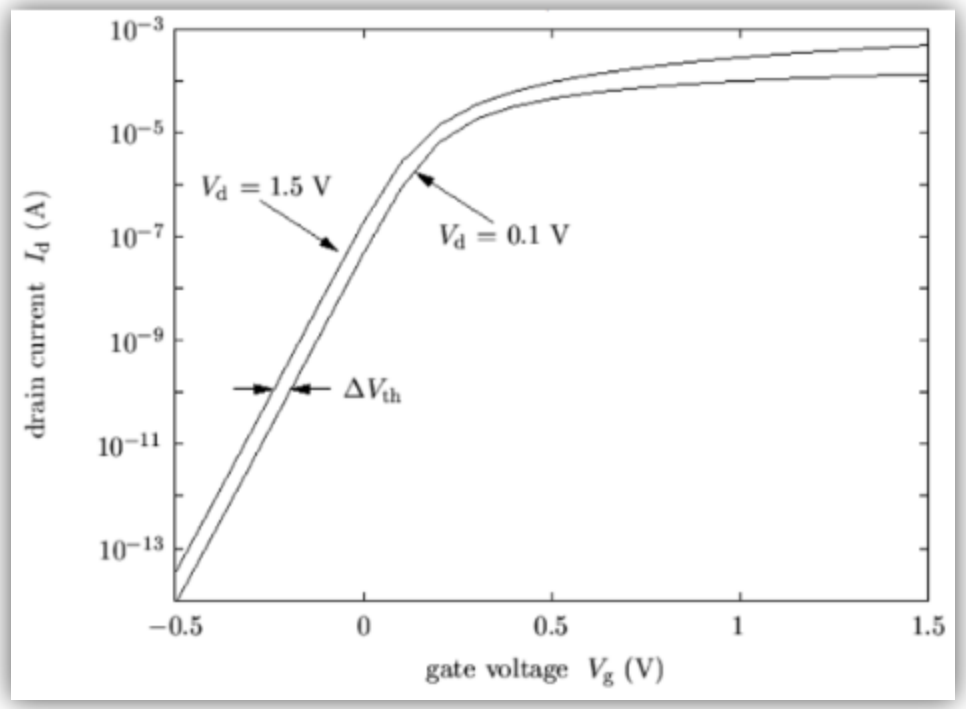
$$I_{D(linear)} = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left[2(V_G - V_T)V_D - V_D{}^2\right]$$

$$\cong \mu C_{ox}\frac{W}{L}(V_G - V_T)V_D \quad (\text{if } V_D \sim 0)$$

$$\Rightarrow \text{Linearly extrapolated } V_T$$

Characterization Calculation

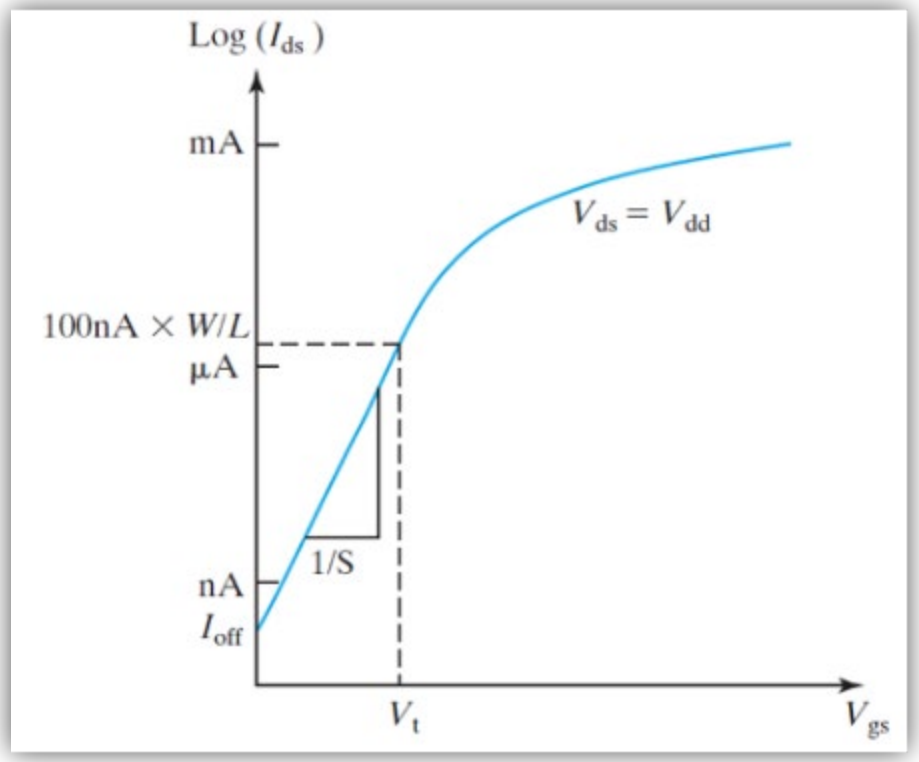
- Drain-Induced Barrier Lowering (DIBL)



$$DIBL = \frac{dV_T}{dV_D} \quad \mathrm{mV}/\mathrm{V}$$

Characterization Calculation

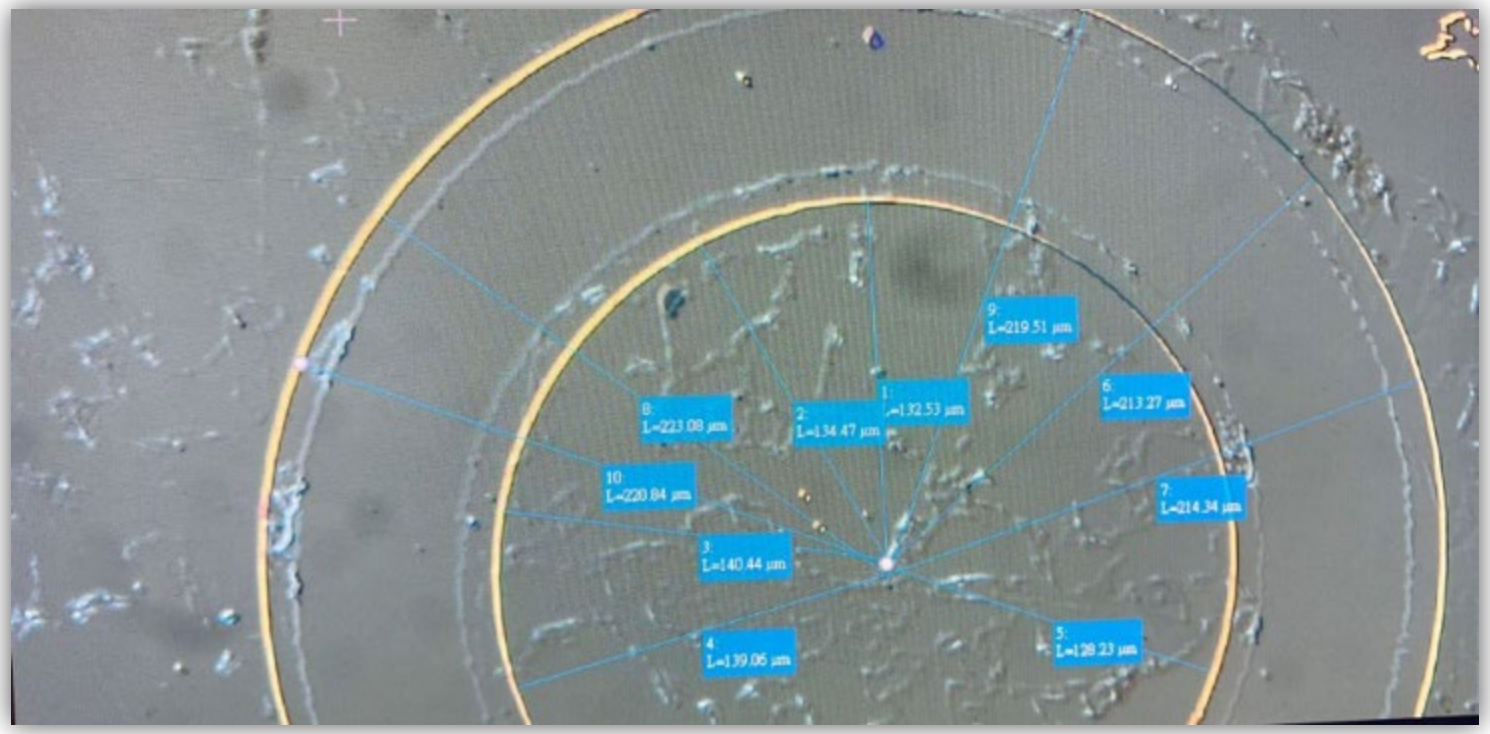
- Subthreshold Swing (SS)



$$\text{Subthreshold swing (SS)} = \left[d\left(\log I_D\right) / dV_G \right]^{-1}$$

Measurement – ring pFET

- Size parameter



Average inner circle radius = 134.95 μm

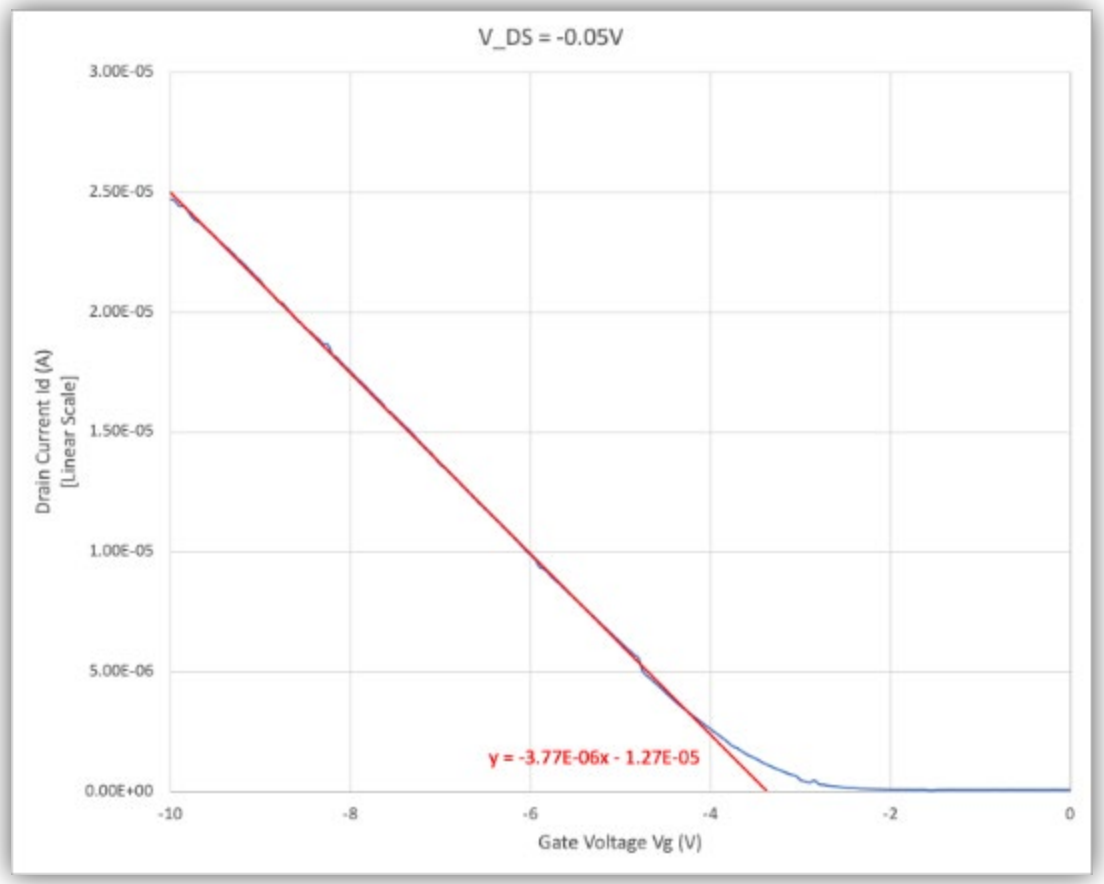
Average outer circle radius = 218.21 μm

Measurement – ring pFET

- Threshold Voltage V_T

  When V_{DS} = -0.05 V

  $\Rightarrow V_T$ = -3.37 V

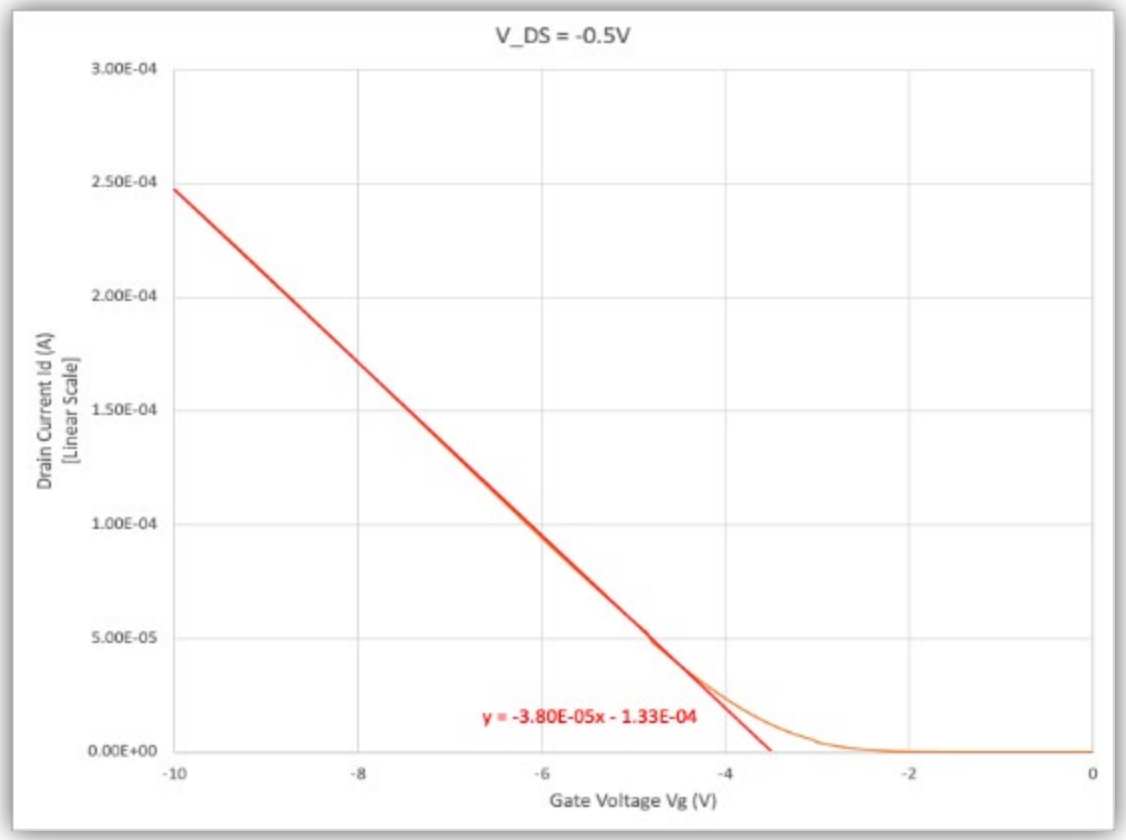


Measurement – ring pFET

- Threshold Voltage V_T

  When V_{DS} = -0.5 V

  $\Rightarrow V_T$ = -3.5 V



Measurement – ring pFET

- Threshold Voltage V_T

  When V_{DS} = -0.5 V

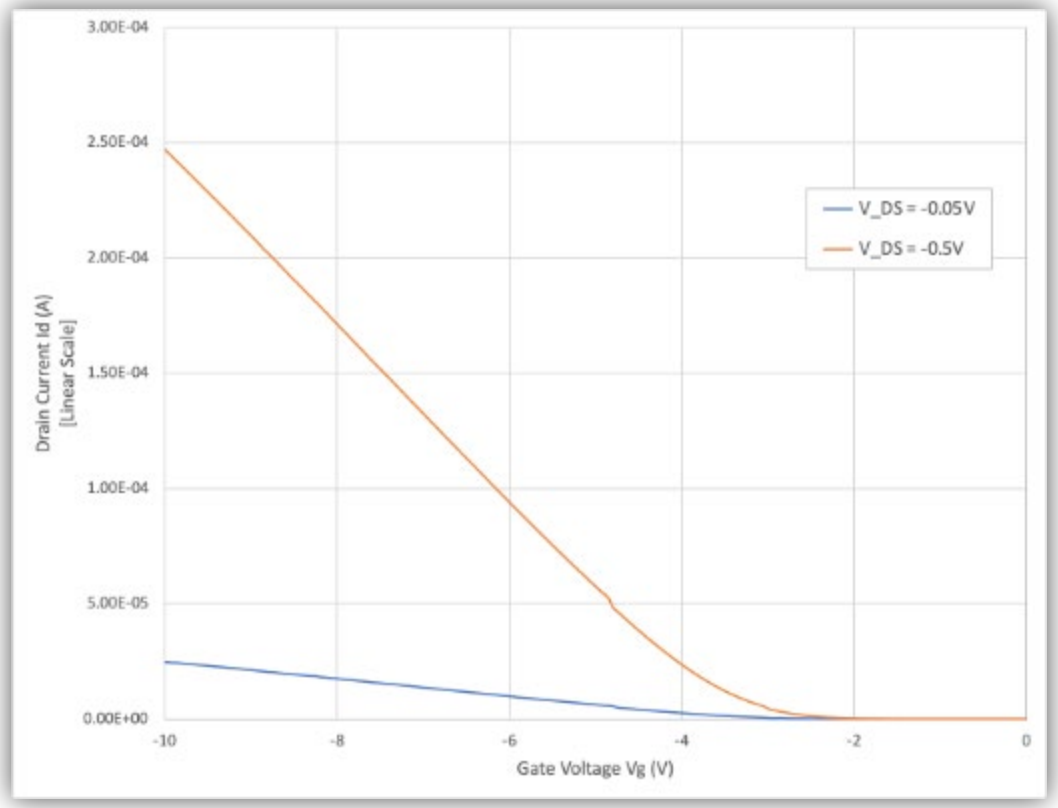
  $\Rightarrow V_T$ = -3.5 V

  When V_{DS} = -0.05 V

  $\Rightarrow V_T$ = -3.37 V

  $\Rightarrow$ DIBL = (3500-3370)/(0.5-0.05)

  = 289 mV/V



Measurement – ring pFET

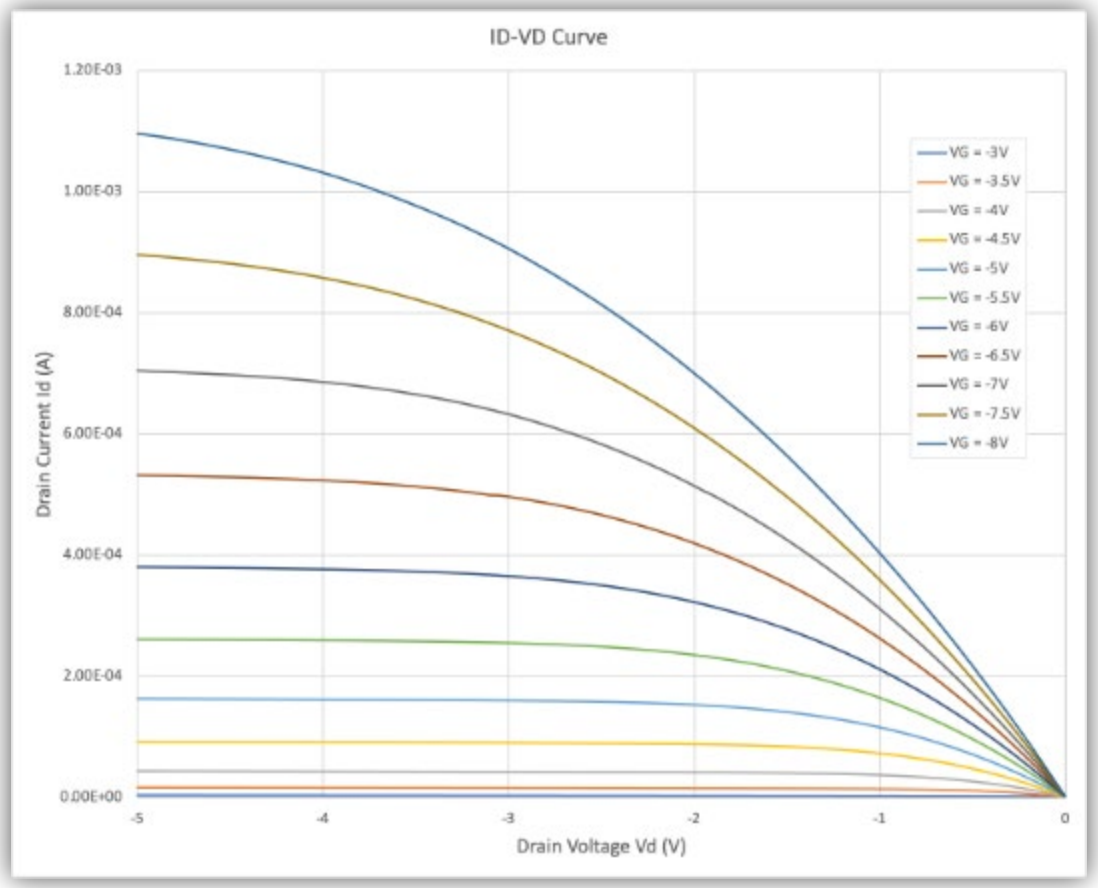
- I_{ON}

  When V_T = -3.5 V

  V_{GS} = -6 V

  V_{DS} = -0.5 V

  $\Rightarrow I_{ON}$ = -350 μA



Measurement – ring pFET

- I_{ON}/I_{OFF}

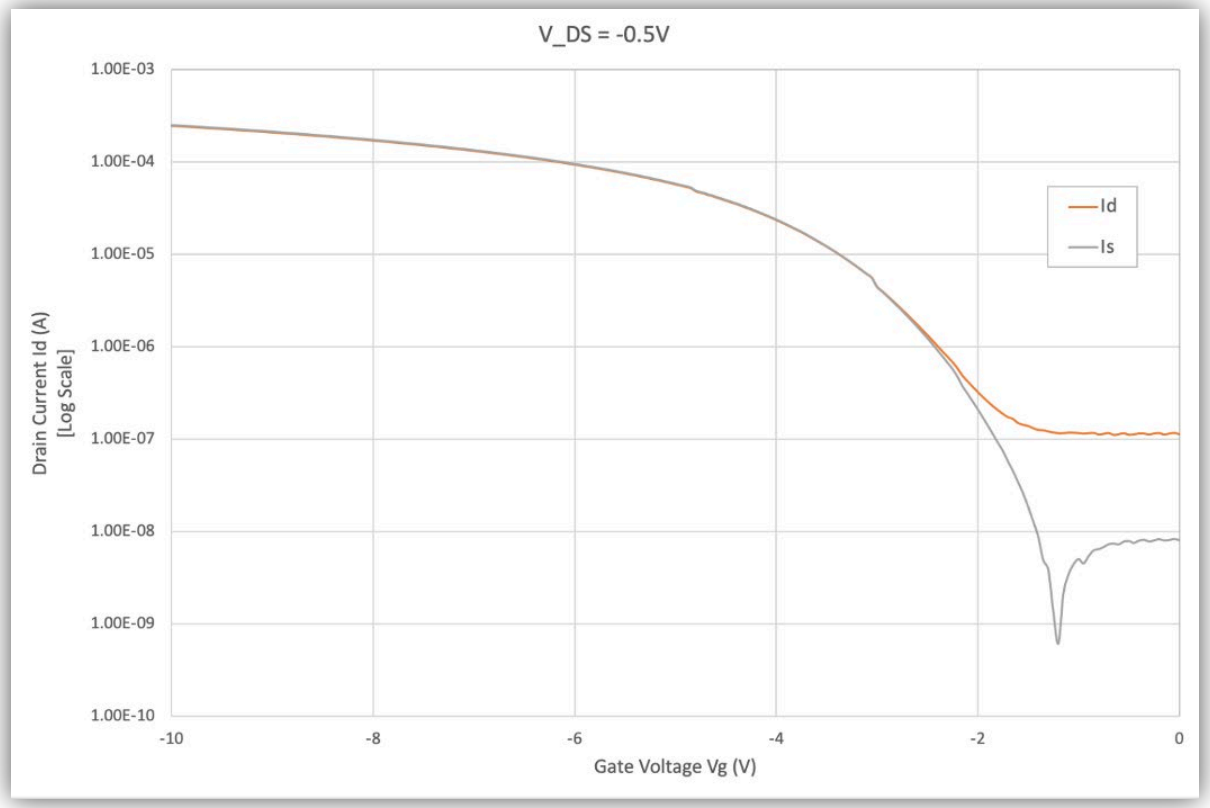
  When V_{GS} = V_T = -3.5 V

  V_{DS} = -0.5 V

  $\Rightarrow I_{ON}$ = 12.1 μA

  $\Rightarrow I_{ON}/I_{OFF}$ = 12.1 μ/0.606n

  = 19667 A/A



Measurement – ring pFET

- Threshold Voltage V_T

  When V_{DS} = -0.5 V

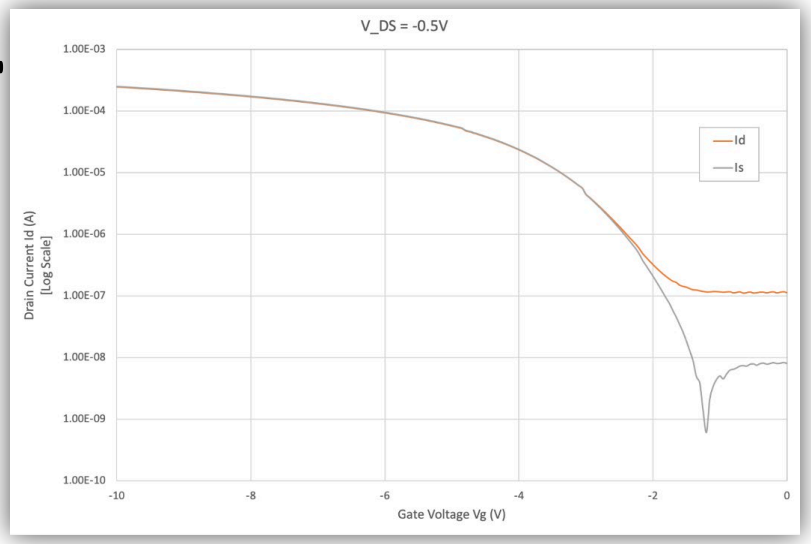
  $\Rightarrow SS$ = {[log(4498n)-log(3262n)]/1000}$^{-1}$

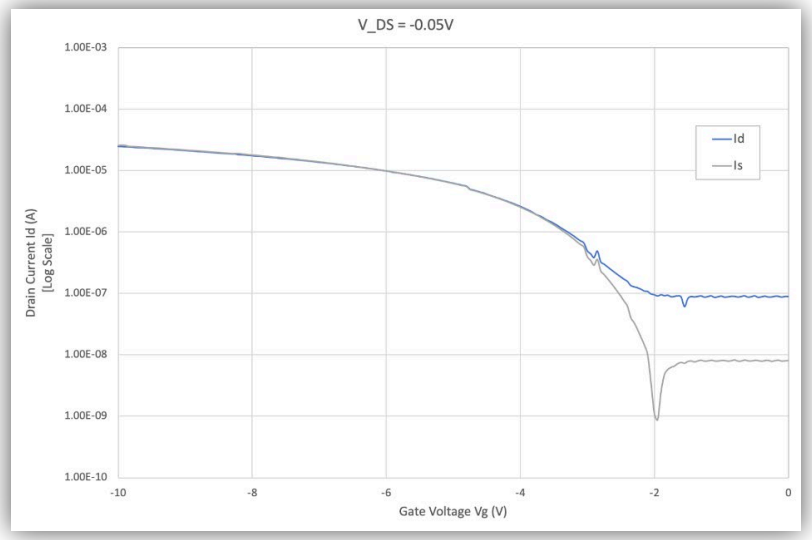
  = 877 mV/dec

  When V_{DS} = -0.05 V

  $\Rightarrow SS$ = {[log(1383n)-log(185.6n)]/1000}$^{-1}$

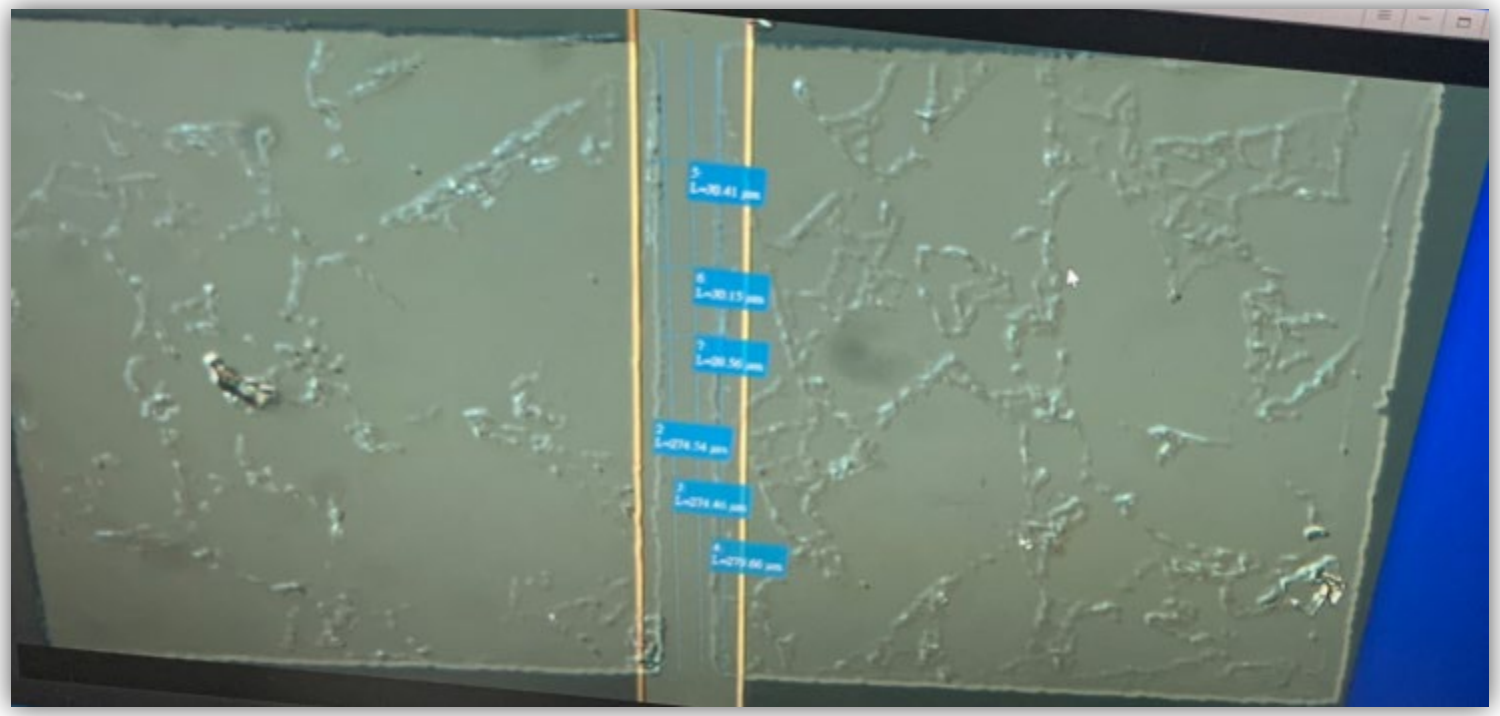
  = 1146 mV/dec





Measurement – rectangular pFET

- Size parameter



Average L = 29.7 μm

Average W = 276.22 μm

Measurement – rectangular pFET

- Threshold Voltage V_T

  When V_{DS} = -0.5 V

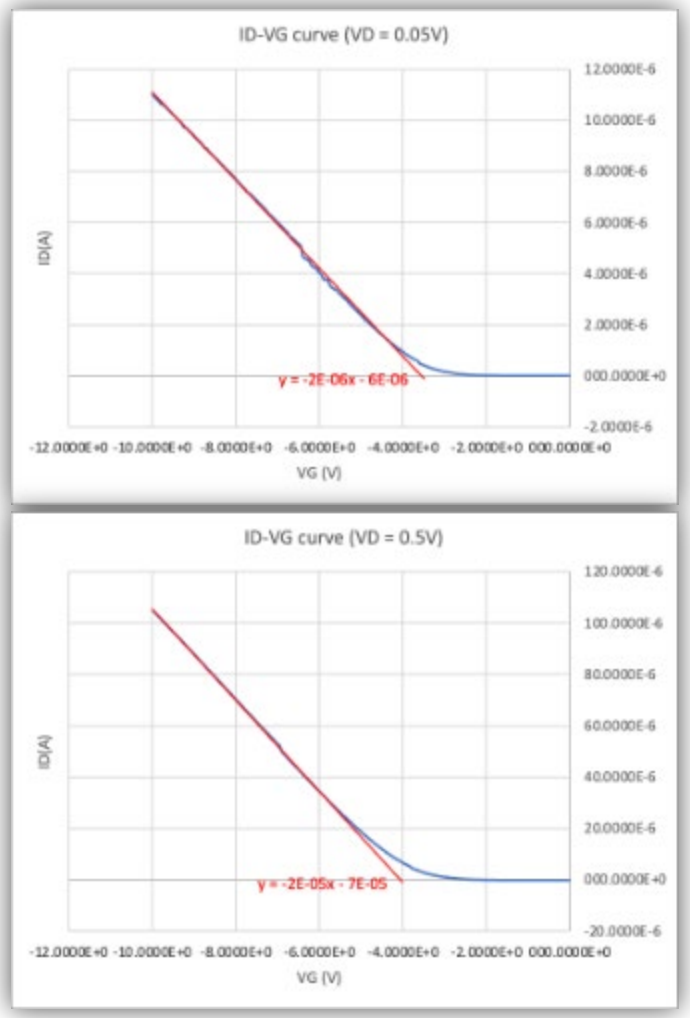
  $\Rightarrow V_T$ = -3.5 V

  When V_{DS} = -0.05 V

  $\Rightarrow V_T$ = -3 V

  $\Rightarrow$ DIBL = (3500-3000)/(0.5-0.05)

  = 1111 mV/V



Measurement – rectangular pFET

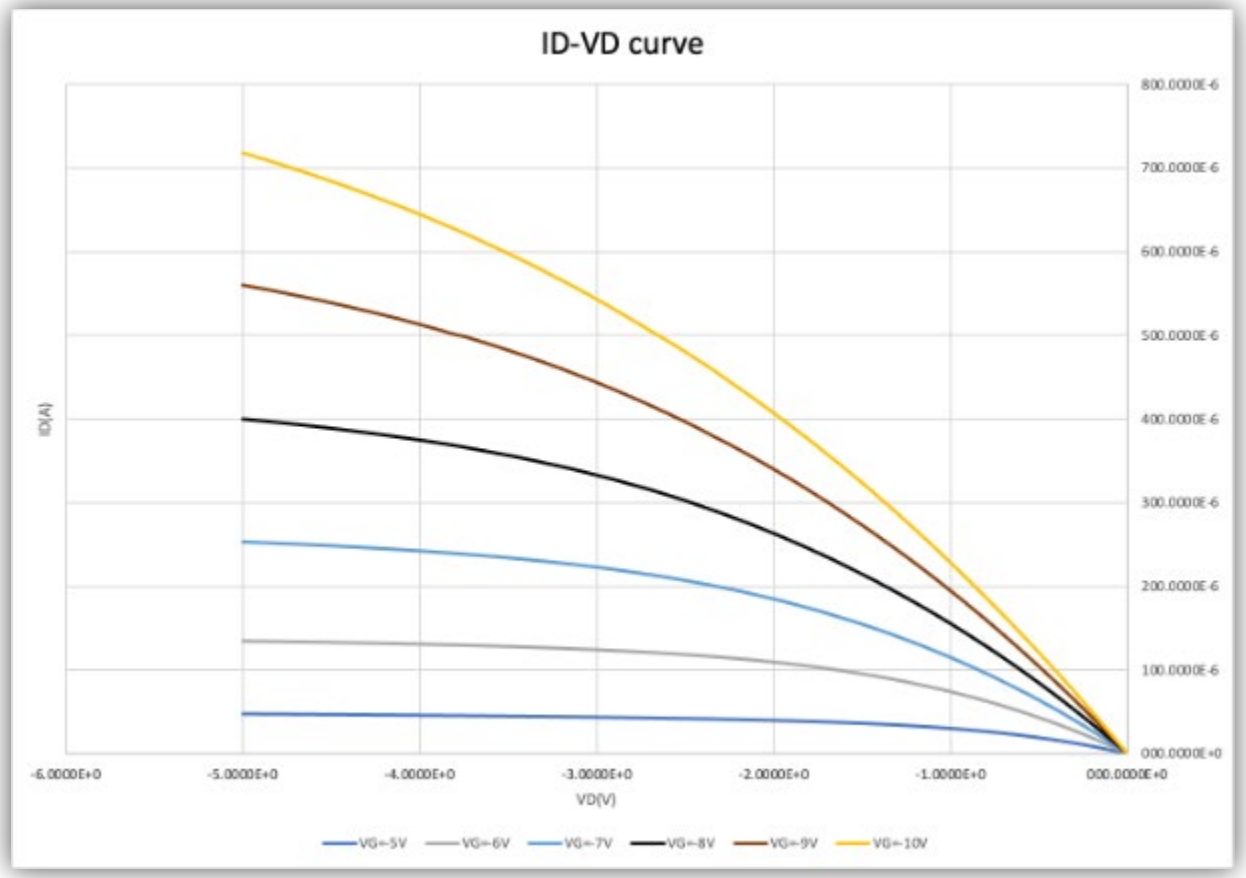
- I_{ON}

  When V_T = -3.5 V

  V_{GS} = -6 V

  V_{DS} = -2.5 V

  $\Rightarrow I_{ON}$ = 77 μA



Measurement – rectangular pFET

- I_{ON}/I_{OFF}

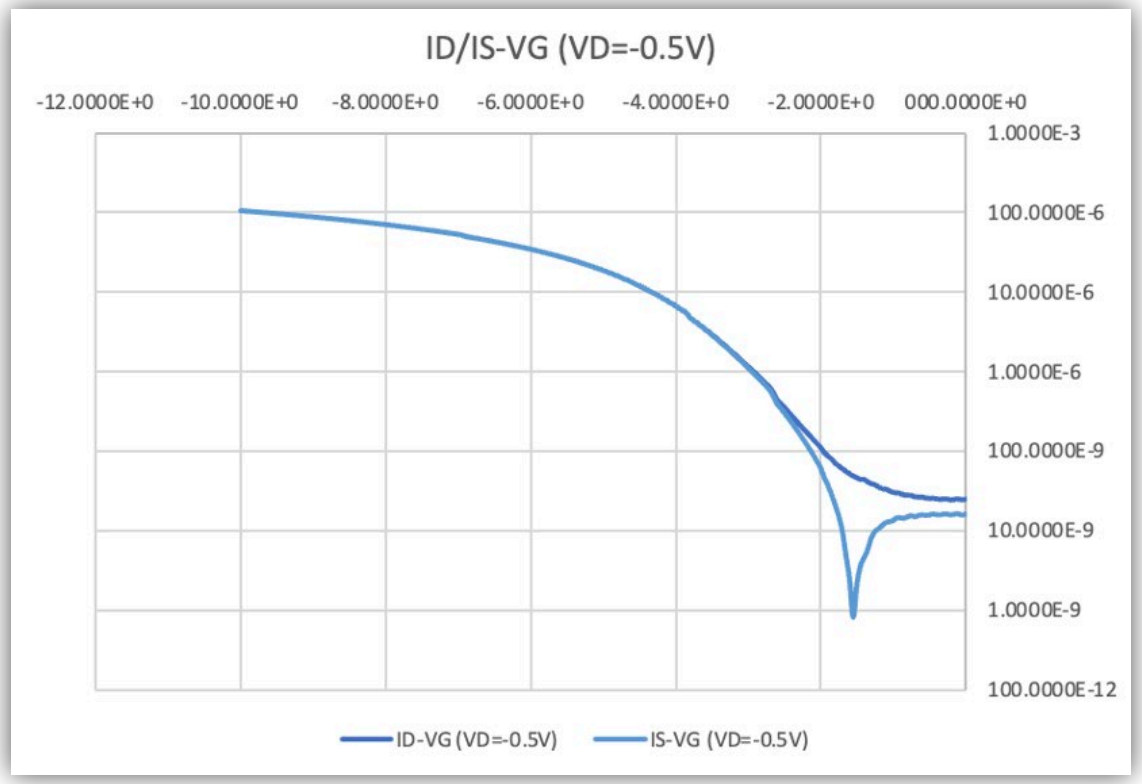
  When $V_{GS} = V_T$ = -3.5 V

  V_{DS} = -0.5 V

  $\Rightarrow I_{ON}$ = 2.8946 μA

  $\Rightarrow I_{ON}/I_{OFF}$ = 2.8946 μ/2.51n

  = 1153 A/A



Measurement – **rectangular pFET**

- Threshold Voltage V_T

  When V_{DS} = -0.5 V

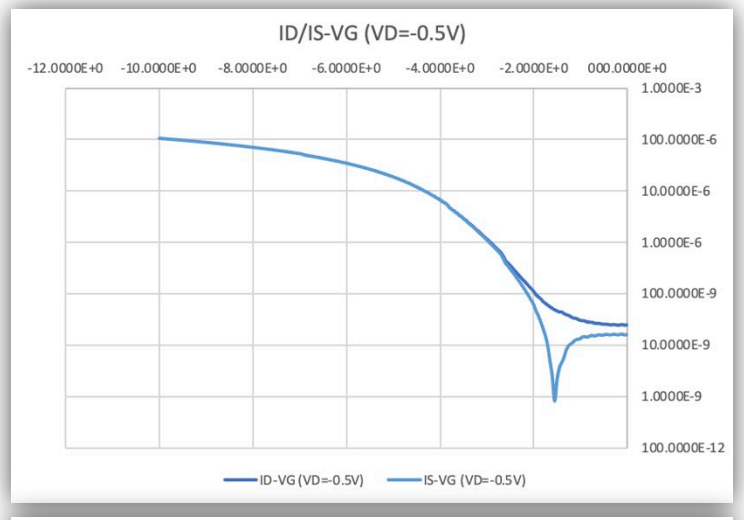
  $\Rightarrow SS$ = {[log(1117n)-log(588n)]/300}$^{-1}$

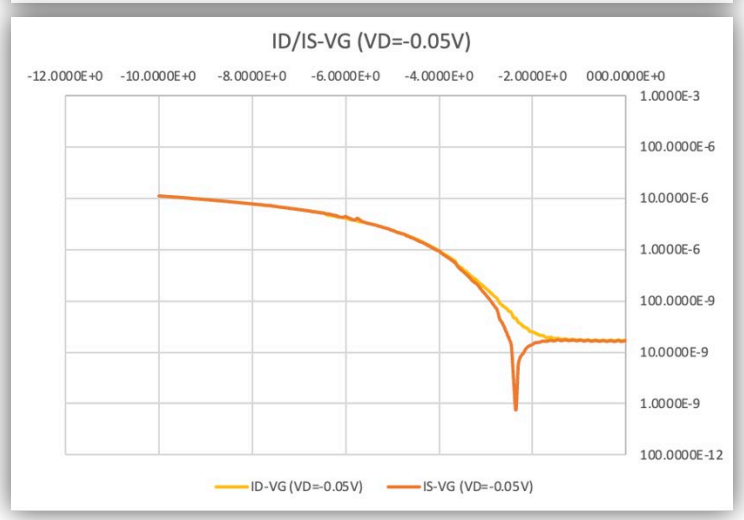
  = 1076.5 mV/dec

  When V_{DS} = -0.05 V

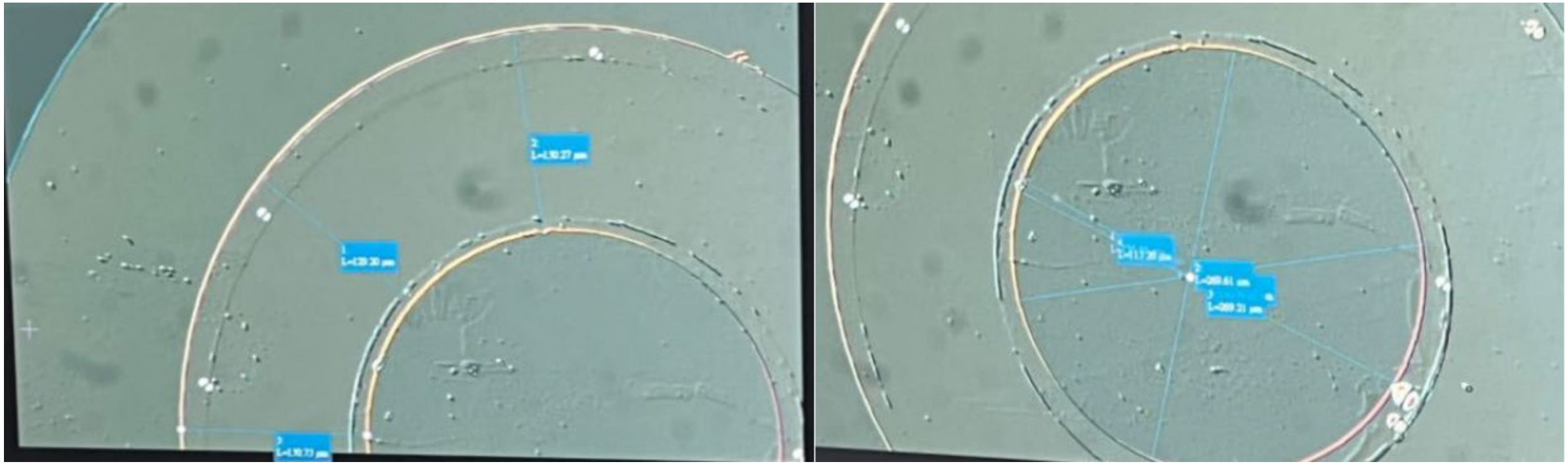
  $\Rightarrow SS$ = {[log(131.1475n)-log(44.0631n)]/300}$^{-1}$

  = 633 mV/dec





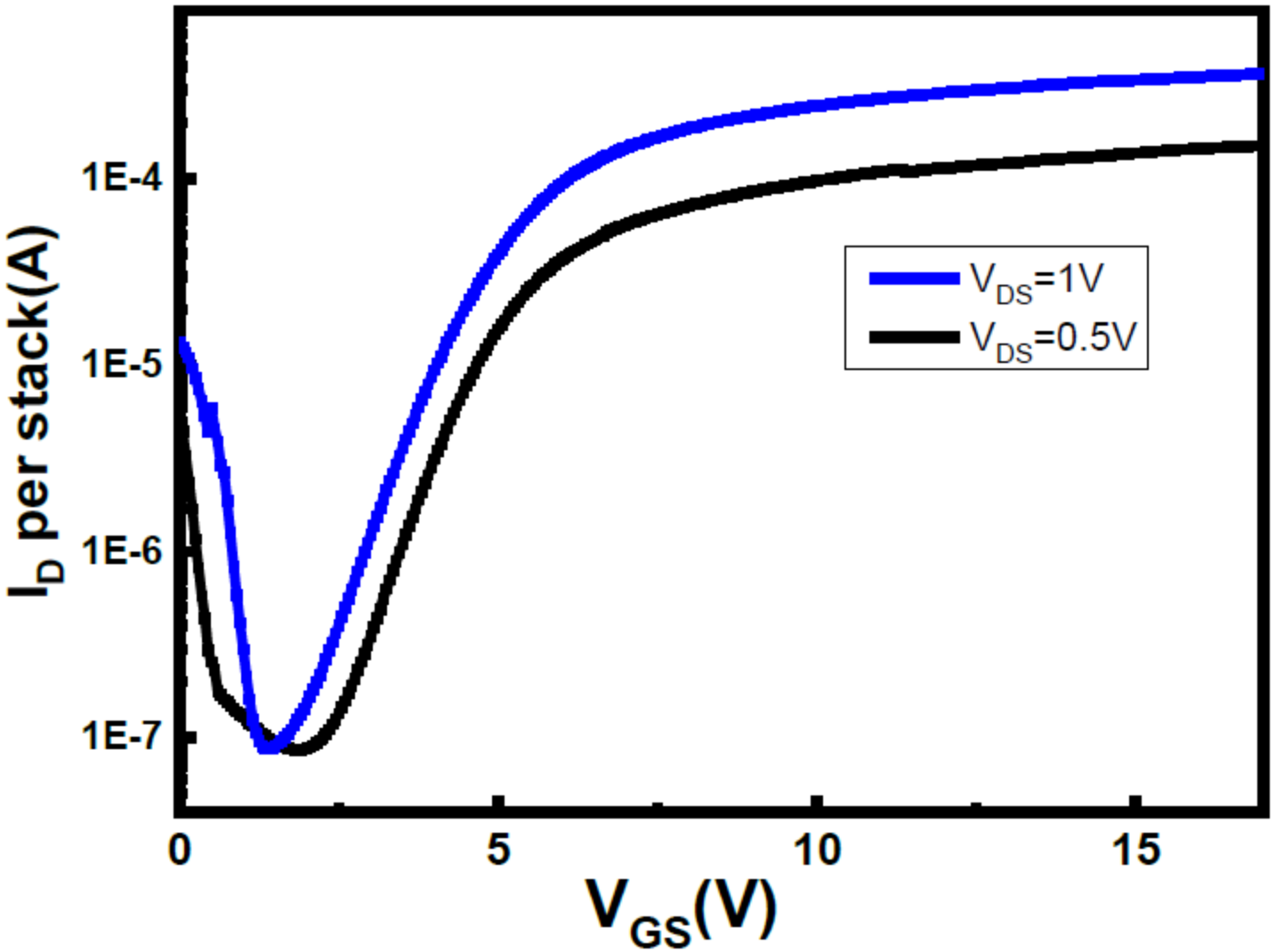
nFET Ring Measurement



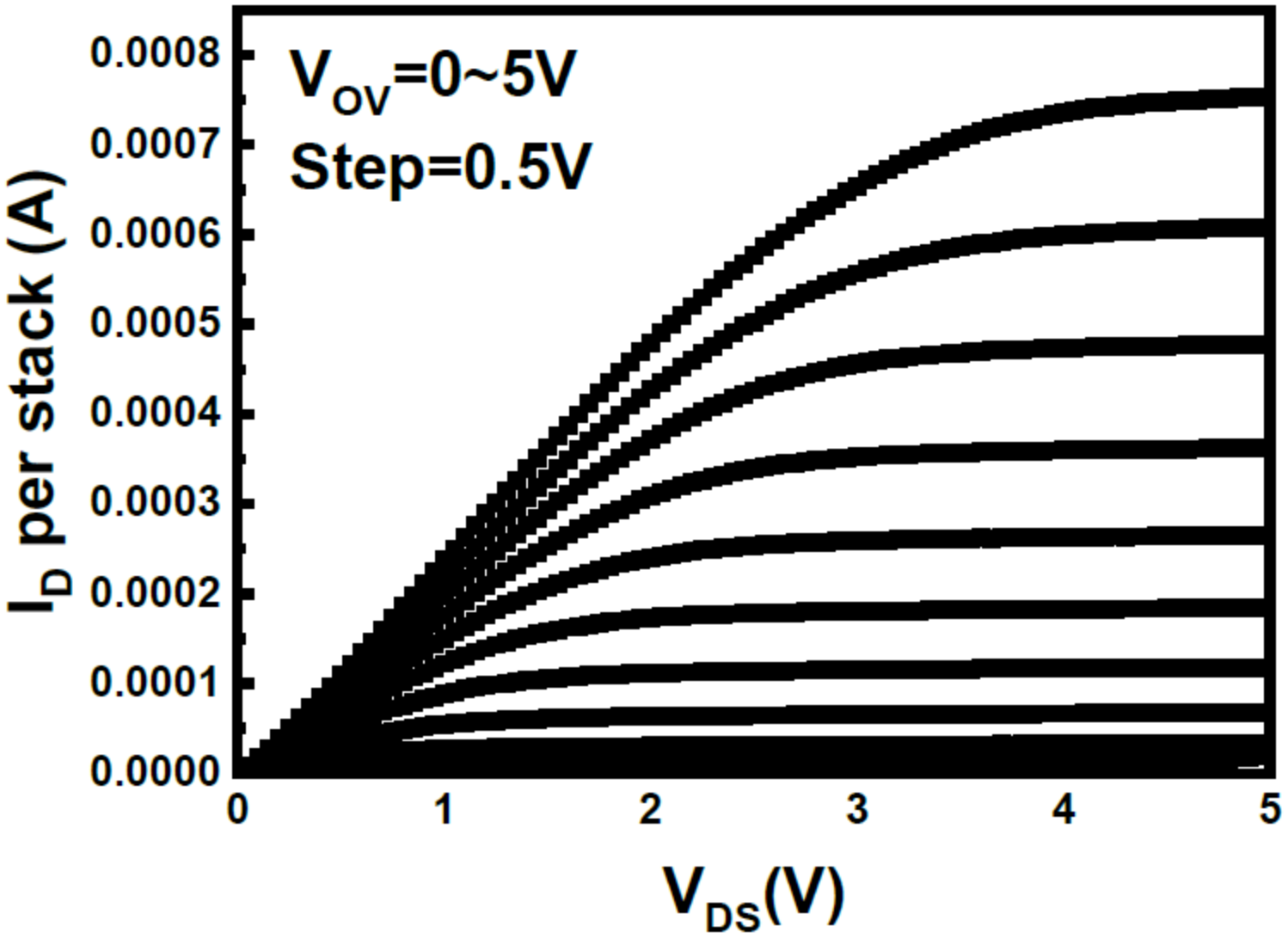
Average inner circle radius = 135 μm

Average outer circle radius = 270 μm

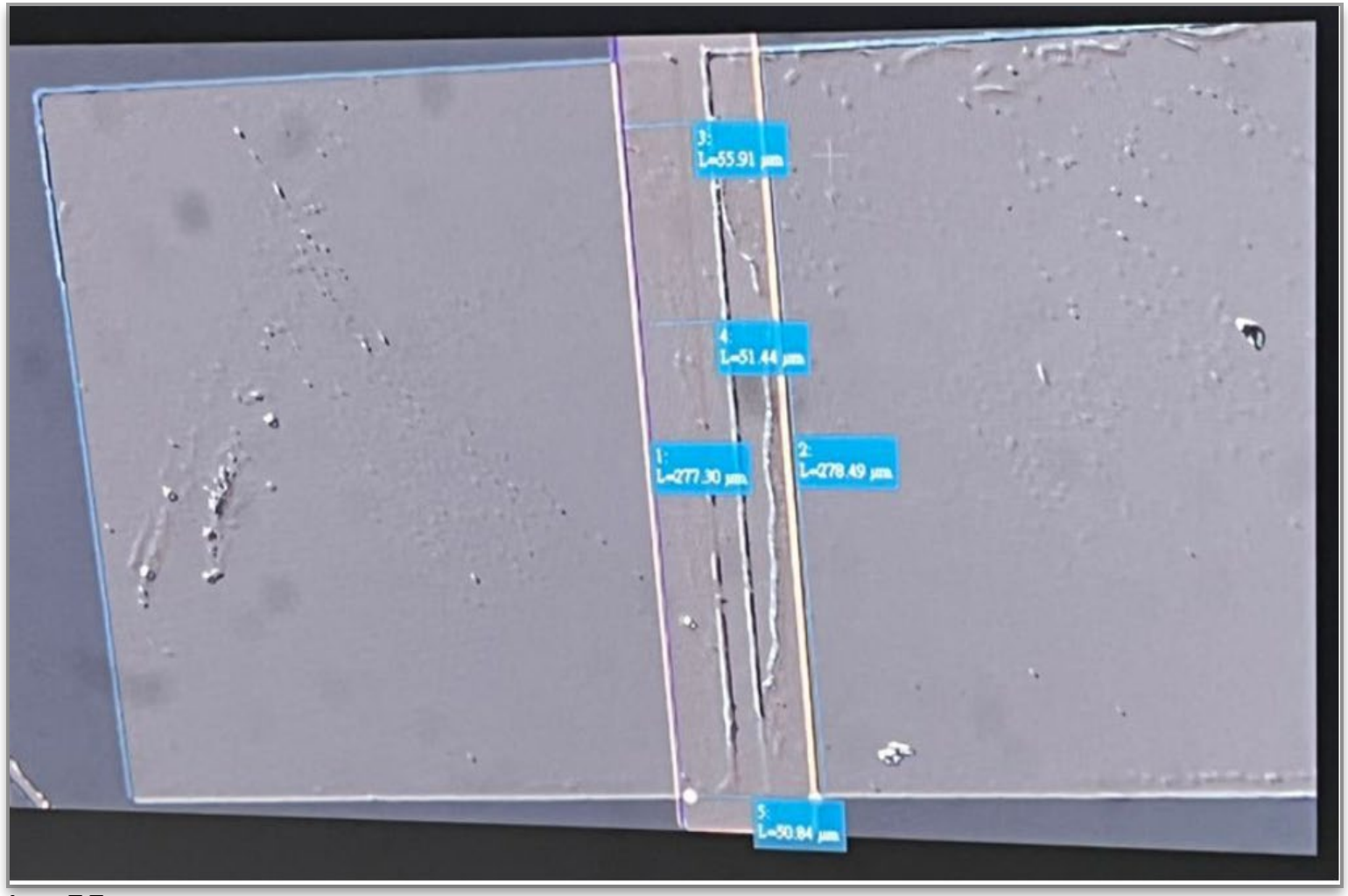
nFET (ring)



nFET (ring)


V_{OV}=0~5V
Step=0.5V
I_D per stack (A)
0.0008
0.0007
0.0006
0.0005
0.0004
0.0003
0.0002
0.0001
0.0000
0
1
2
3
4
5
V_{DS}(V)

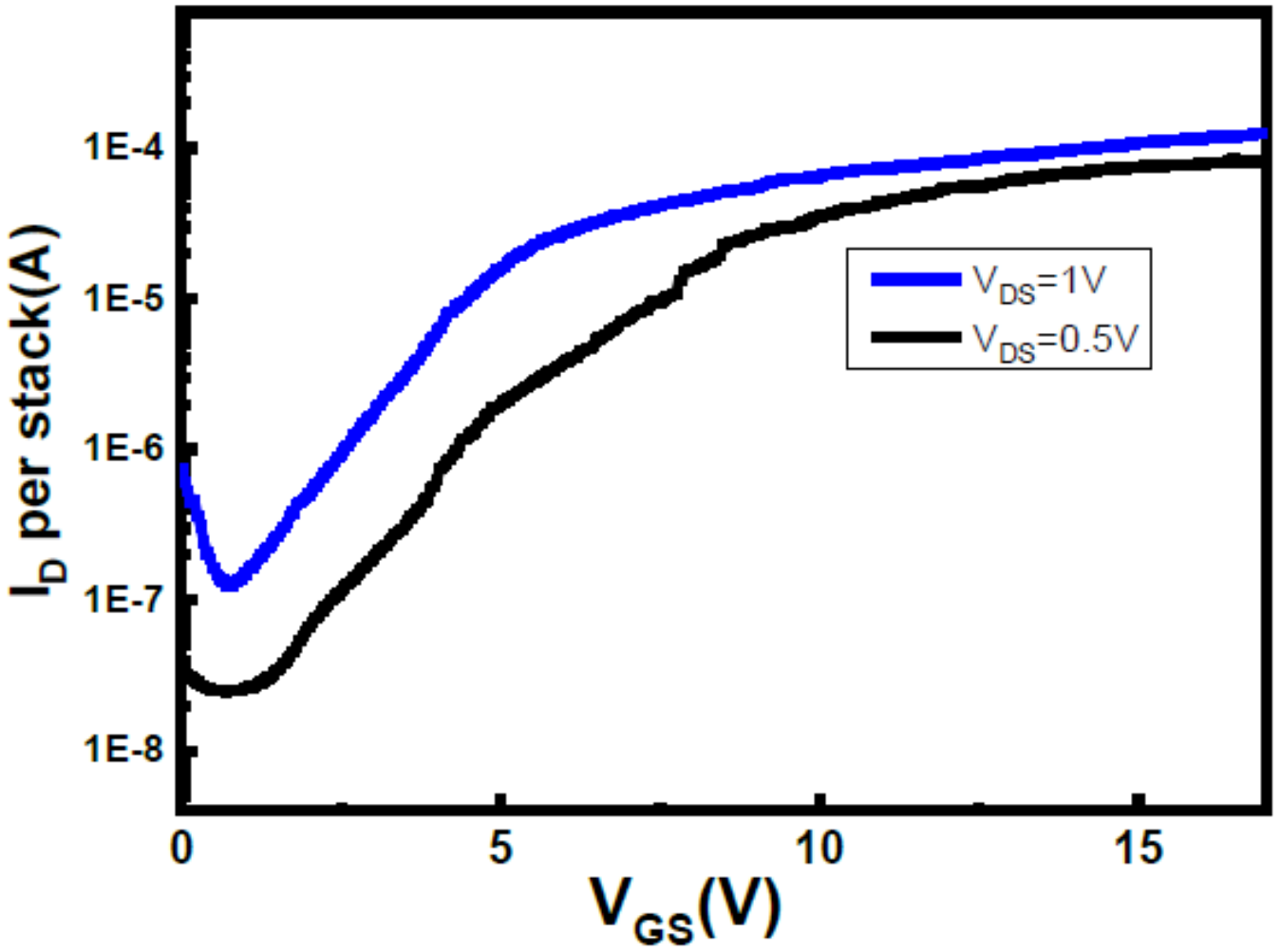
nFET Rectangle Measurement



Average L = 55 μm

Average W = 280 μm

nFET (rectangle



nFET (rectangle)